elektor

6

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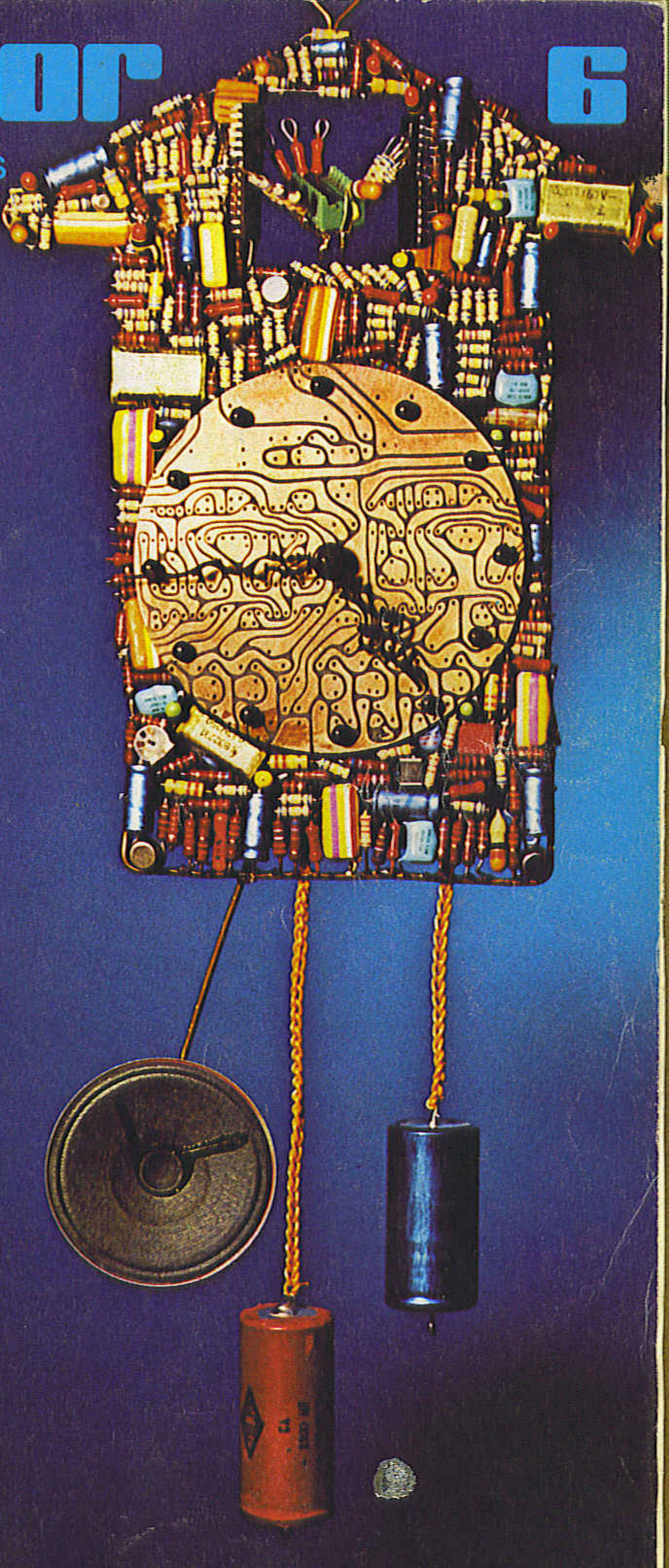

September 1975 35p

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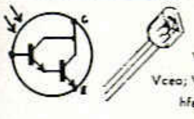

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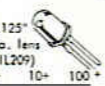

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contents

selektor 905

edwin amplifier 910
This is a design for a high-quality 40 W audio amplifier based on an earlier 20 W design. The amplifier embodies some unusual design features and the construction is problem-free.

miniature amplifier 917
The circuit will operate from a 4.5 V battery and can be used to amplify the output of a crystal pickup to drive a small loudspeaker or headphones. The circuit is not outstanding for its power or quality, but it is simple and reliable.

versatile digital clock 918
'One-chip' digital clocks, such as the MM5314 (Elektor 1, p. 24), are excellent for simple time-keeping. However, they are not ideal for driving external devices such as time signals, calendars, etc. This is where a 'conventional' clock design with standard TTL ICs scores; it has a BCD-coded time output, as well as pulse train outputs giving repetition rates varying from one per second to one per day.

phasing – G. Knapienski and F. Mitschke 922
Nowadays there are a great number of methods of producing unusual electronic sound effects. A favourite effect is 'Phasing' and in this article this is accomplished, somewhat unusually, by using a 'path filter'.

disco lights 924
Various kinds of psychedelic flashing light display can be generated easily using logic shift registers. Several circuits are discussed here of varying complexity.

ota 927
The OTA (Operational Transconductance Amplifier) is a new type of operational amplifier. The gain can be determined externally by the value of the output load resistor, and by the so-called bias current. The latter makes it possible to control the gain instantaneously over a range of about 80 dB by an external potential. Since the OTA will be used in several Elektor projects, an explanation of the working principles of this device should prove useful.

fish feeder – F. Sax 931
The care of aquaria during holidays can be something of a problem. However the device described here will overcome this problem by automatically dispensing the required quantity of feed each day.

tri-stable – J. Koper 933

roll out the bandit – L. Wiechers 934
The disadvantage of the 'three-eyed bandit' (Elektor No. 2 page 238) is that a stop button must be pressed to stop the three oscillators and obtain the final display. Thus the tension and anticipation obtained with a real one-armed bandit as the number drums slowly grind to a halt is missing. The circuit described here overcomes this by providing an output whose frequency slowly reduces until it finally stops.

light dimmer 935

dual slope dvm – H.L. Krielen 936
A design is described for a basic 2½ digit digital voltmeter using the dual-slope integration principle. The DVM has a full-scale sensitivity of 199 mV, but may be extended at the constructor's option.

lep – A. Schulz 942
A LEP (light emitting pistol) with electronic time and hit indication offers the possibility of moving the age-old fair attraction 'the shooting stall' to the living-room.

bicycle trafficator – N. Beun 944

30 mhz amplifier – W. Kümmel 945
The input threshold voltage of TTL IC's lies between 1.8 and 3 volts. This simple transistor amplifier can be used to amplify relatively low-level signals to a level suitable for driving frequency counters and other equipment.

car clock 946
The Eurosil E1109IC offers the possibility of a single-chip digital clock operating directly from a crystal reference. Using this IC a compact clock can be constructed which is eminently suitable as a car clock or portable clock.

market 949

the missing link 952

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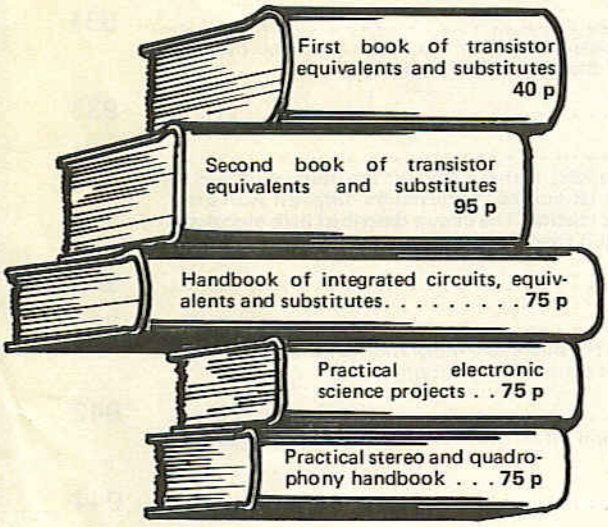

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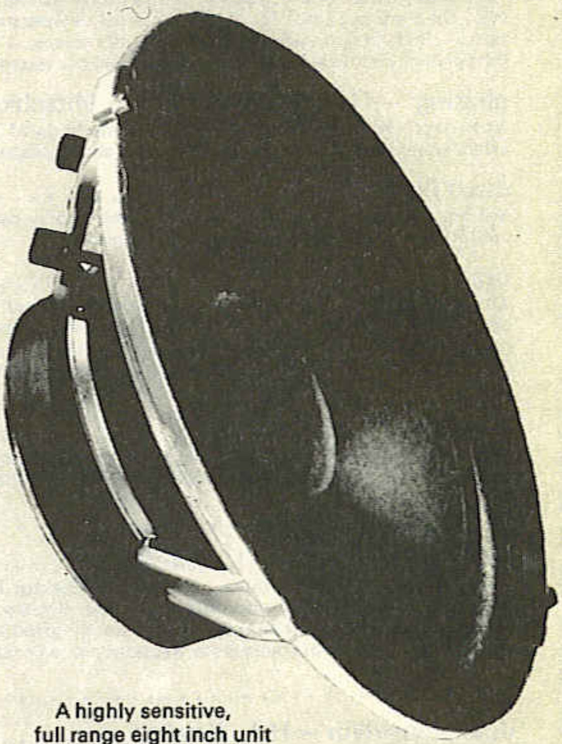

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selektor

Automatic tester for mono and stereo broadcast circuits

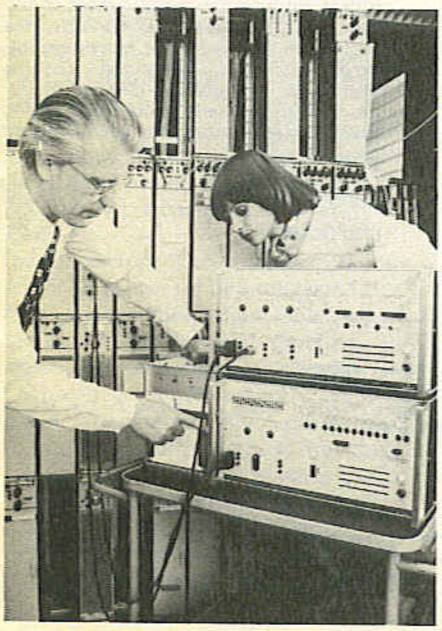
For regular interchange of programmes, broadcasting organizations use special programme circuits placed at their disposal by the telephone administrations either as permanent connections or, if they cross national borders, as temporarily established transmission paths. Until now, assessment of the quality of such circuits was performed manually and met with some difficulties, especially in the case of international programme transmission (non-uniform test methods, different test instruments), as well as being unsatisfactory with regard to the time required for lining-up. With automatic tester K 1060, Siemens are now offering an instrument for automatic quality supervision of mono and stereo programme circuits.

The automatic tester, designed according to the most recent CCITT recommendation for programme circuits from 30 Hz to 16 kHz, consists of a transmitter and receiver, each containing a test and control unit, and a high-speed recorder. Among other things, the weighted (psophometric) and unweighted noise, non-linear distortions, level step, frequency response, level difference and sum level, phase difference and crosstalk can be assessed. Two main routines (mono and stereo) and nine sub-routines are available. The automatic test routine for mono circuits, including printout of the record, takes only about 133 seconds, while that for stereo circuits takes about 370 seconds.

The test unit of the *transmitter* contains two spot-frequency generators and a function generator which supplies various spot-frequencies at certain input voltages; a frequency sweep from 30 Hz to 16 kHz is achieved by using a variable dc voltage. This dc voltage increases exponentially, producing a logarithmic frequency sweep. In addition to this, beginning at 50 Hz a pulse is added to the signal at each octave, the recorder registering the pulse as a frequency marker. The output voltages of the three generators are supplied individually or in a combination, depending on the test mode, to an amplifier; they are then set automatically by means of variable attenuators to the exact value required in each case. The outputs for channels A and B are balanced and floating. For monitoring purposes, the test routine in progress can be followed over the built-in loudspeaker or over earphones. The control unit of the transmitter, which is equipped with a clock generator, is used for automatic step-by-step execution of the test routine.

The test unit of the *receiver* has two balanced floating transformer inputs of identical design for channels A and B. The test circuit for channel A has attenuators in front of and behind the amplifier which can be cut in automatically according to the test mode. These are followed by various filters for weighted and unweighted measurement of noise, non-linearity and crosstalk. The signal is applied via a further amplifier to the rectifier, whose output voltage is passed through a logarithmic network to obtain level-linear indication on the recorder. Here again, the test routine can be monitored over the built-in loudspeaker or over earphones. The test circuit for channel B is similar in design to that for channel A. As in the case of the transmitter, the control circuit of the receiver is equipped with a clock generator, and in addition to this it has automatic start-signal selection facilities.

A high-speed recorder is connected to the output of the receiver to record the test result. The utilized recording width is 100 mm, corresponding to a range of 20 dB for level measurement and 50 angular degrees for phase-difference measurements.



Modem without modulation

For the transmission of data signals over switched telephone networks, modems are used to modulate the dc signals on the send side and to demodulate them on the receive side. If dedicated circuits are used, however, which is especially favourable over short distances - in conurbations for example - transmission equipment can be used which operates without modulation and which is therefore less complex. One device of this kind is the Modem N10 developed by Siemens, which uses direct-current keying for transmission.

The Modem N10 is suitable for data transmission over metallically coupled two - or four-wire lines at bit rates of up to 9600 bit/s. The device has no fixed code or speed and permits all conventional operating modes — simplex, half-duplex and duplex operation. This last mode is also possible over two-wire lines, which substantially reduces line costs. The maximum range is rated - depending on operating mode and speed - at almost 30 km. Under adverse operating conditions and with a bit rate of 2400 bit/s the error rate is only 10^{-8}, i.e. out of 100 million characters one may be falsified.

The device may also be used for multipoint operation. In this mode, one control station transmits over only one line to a number of outstations. A station address is previously specified, so that the message is only evaluated by the data terminal for which it is intended; if necessary, this can then return an answer to the control station. The operational integrity of the Modem N10 can be checked at any time with the aid of the built-in test facility without further aids. The interface to the data terminal corresponds to the relevant CCITT Recommendations, so that the modem can interoperate, without matching problems, with the same data terminals as the modems employed for the speed range up to 9600 bit/s over switched telephone circuits.

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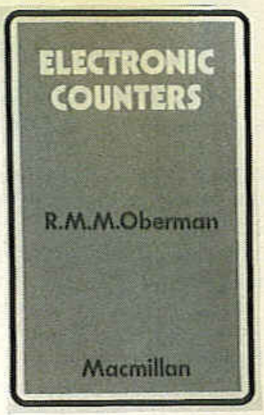

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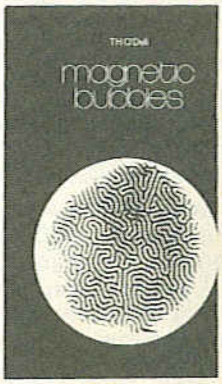

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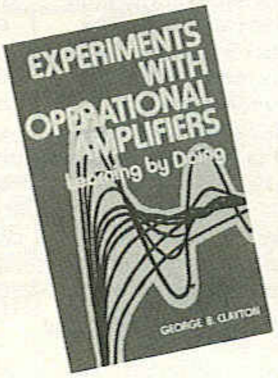

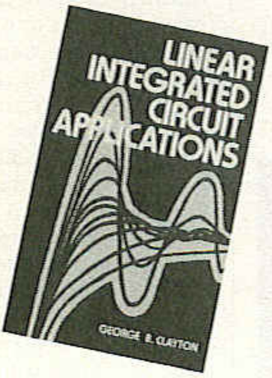

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This book is concerned with the newer circuits now available, important for such things as signal measurement and processing systems.

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New mounting technique ensures high-reliability circuitry

In the past, there has been no lack of effort to find an economical and reliable way of replacing the conventional system of wire connections currently used in semiconductor production. AEG-Telefunken have now succeeded, with their 'Sicon' process, in developing a technology which cuts out the hitherto-unavoidable human factor and reduces the cost of the 'connection' stage in the mounting process to a mere 11% of what it was before. In a second stage of development it should be reduced to 5%.

The starting point in the new mounting process is the use of a new metal alloy, different from those used in current metal-plating processes, for plating the connection-points on the active element.

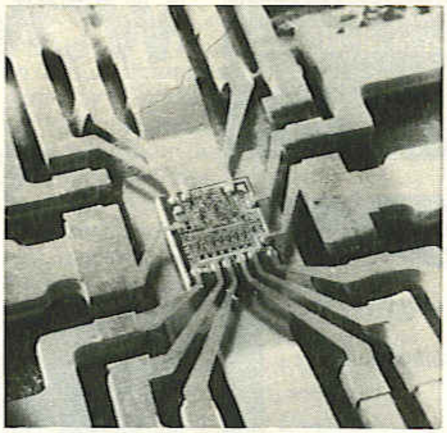
○ Aluminium plating is replaced by a heavy-metal contact system based on an alloy of titanium (Ti), tungsten (W for wolfram) and gold (Au).

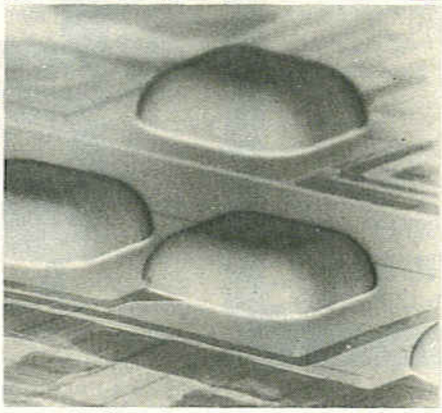
○ Gold balls are 'grown' electrolytically on the contact-point areas of the semiconductor chip.

This process has largely eliminated 'purple plague'* and has achieved a minimal degree of electron migration.

In contrast to all other techniques so far known, the die is directly bonded with the body of a dual-in-line strip via an intermediate layer having a good thermal conductivity. For the connection between die and body a nickel-plated spider is used. This is held in a frame, which is in turn fixed by four narrow transverse bands. Since the spider is accurately positioned with respect to the die and the positioning of the frame to the dual-in-line body is relatively problem-free because of the much larger contact surfaces, displacement of the die up to about 150 μm from its design position in either the X- or the Y-direction becomes permissible. The electrolytically-plated gold balls, together with the latitude permitted by the spider, preclude the occurrence of displaced bonds.

The robustness of the connections in the Sicon process is demonstrated by their high breaking strain. This averages about 50 p and represents an improvement of about ten to one, if the average figure currently achieved with a wire diameter of 25 μm is taken as a basis for comparison. A breaking strain of this magnitude ensures that mechanical strains, occurring at later stages before the mounting process is completed, will not destroy the connections. In the initial basic research, a temperature cycling test over a range of +110° C to -195° C was carried out, with a time of 30 seconds between successive maximum temperatures; this goes far beyond the demands occurring in normal use. This degree of severity was chosen for the stress-testing because, with the usual range of temperature variation from - 40° C to +125° C, no failures at all were found to occur with the Sicon process. While 50% of modules with normal wire connections had already failed after 2100 test cycles, the corresponding figure in the Sicon process was 400,000 cycles.





The Sicon process not only sets new standards from a technical point of view; it does the same from an economic point of view. In one test, for example, the rate of production of integrated circuits was stepped up from 65 to 1000 units per hour. Production costs fell to about a tenth of their previous level.

New laser trim system with self-teaching software

Boston,MA-Teradyne, Inc. has introduced the computer-operated W211 Laser Trim System for the trimming and testing of thick and thin film resistors on silicon, ceramic, sapphire, or glass. The W211 performs functional trimming to voltage, current, and frequency, as well as trimming to a specific resistance.

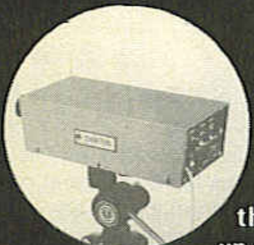
The software supplied with the W211 allows a programme to be generated simply by answering questions displayed on a CRT terminal. Typical questions include the number of resistors to be trimmed, their values, pin connections, type of cut desired, etc. No formal programme training is required.

The W211 includes a control group, a measurement group, a single trim station, and an in-line handler. The control group includes a computing controller, a data terminal, and a magnetic tape unit. Trim limits can be programmed to a resolution of .1% of range. Ranges are 20 ohms full scale to 20 megohms full scale in decade steps.

The trim station has a YAG laser, high-speed galvanometer, beam positioner, and laser station control. Options include a rotary or step-and-repeat handler, and viewing optics. The system can be converted in the field into full W311 Laser Adjust System with multiplexing capability.

Data displayed on the CRT display terminal include pretest and final-test results and job-summary sheets.

'Purple Plague' refers to the formation of an intermetallic compound based on aluminium and gold.



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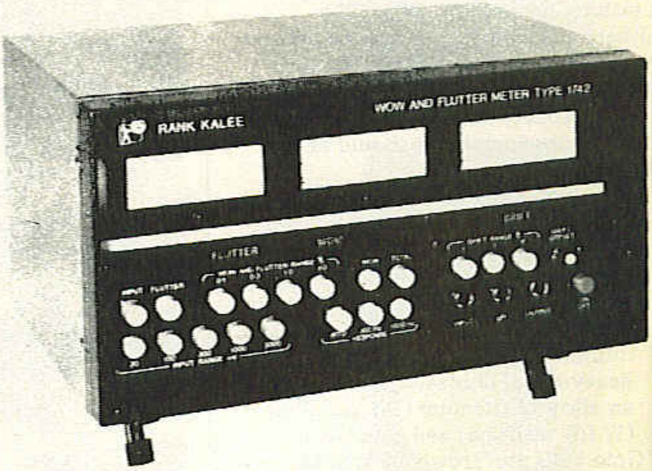

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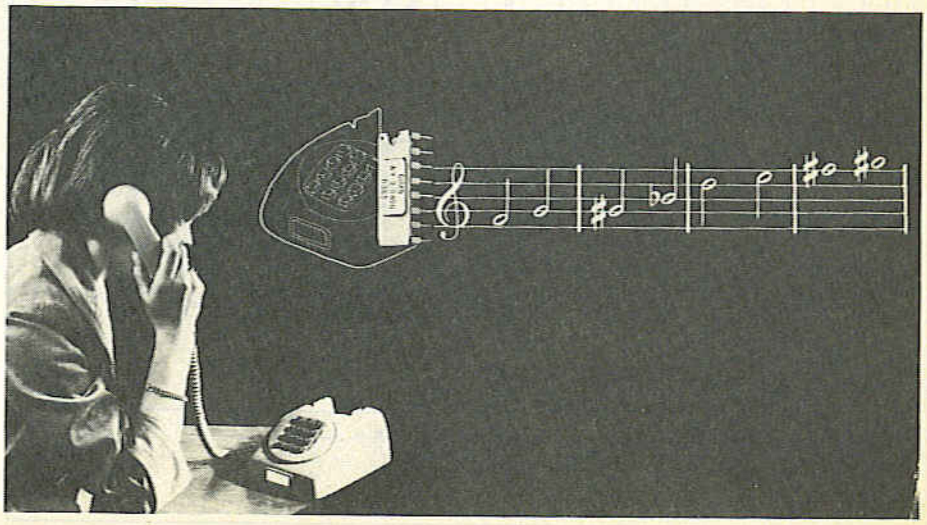
The equipment is safe as it is powered by high-frequency, low-voltage inverters, thus avoiding the dangers associated with conventional high-voltage cold-cathode equipment.

The Effelsberg Radio Telescope — a partial flop?

The latest investigation by the Max Planck Institute for Radio Astronomy into the new 100-metre radio telescope at Effelsberg in the Eifel district of Germany has shown that this complicated space-research instrument has not achieved what the technicians expected of it. This information comes from a recent issue of the technical periodical NTZ. According to this publication, the actual working area of the parabolic antenna has been shown from measurements to be 30% less than was calculated. The reason for this seems to be that the supports for the main focusing cabin, in which the incoming rays are collected, throw too big a 'shadow' on the surface of the parabola. As a result, part of the parabolic antenna remains ineffective. In the future, this problem will be eliminated by a more efficient construction. This, however, will come too late to be of use in the Effelsberg telescope.

First multi-frequency telephone push-button microcircuit

A new MOS microcircuit that can be directly interfaced with a multifrequency telephone key-pad in order to generate the 16 tone pairs used to set-up calls or transmit data, has been designed by General Instrument Microelectronics at their Glenrothes, Scotland, production unit and is now entering production there.
Their new MF telephone key-pad microcircuit, the first to be announced as a standard circuit, represents a considerable advance over conventional tone-generation modules using discrete components and analogue circuit techniques. Greater tone precision, lower assembly and set-up costs, smaller size, lower current drain and a greater reliability are all provided by the new AY-5-9400 which employs an original tone synthesis technique, now patented by the company.
The new microcircuit is expected to arouse considerable interest, particularly in North America where high-speed MF call set-up is standard. For other countries including the United Kingdom and Europe where Strowger or step-by-step dialling is the common practice GIM's AY-5-9100 family of push-button microcircuits is used. These circuits have already become an industrial standard.
In a multi-frequency telephone signalling network the call set-up is accomplished by means of four high and four low tones which can be paired in 16 high-low combinations to represent ten keyed numbers and, in data telephones, six additional control functions.
These tones are generated in a conventional MF push-button telephone by a printed-circuit module incorporating two large coils and a dozen or more active and passive components. Now, the entire module can be replaced by a single MOS LSI microcircuit tacked on the back of a key-pad together with an inexpensive ceramic frequency reference and one or two additional components.
The accuracy of frequencies generated by the MOS-Ceramic tone generator is 1 per cent, well within the 1.5% specification laid down by Telecommunications Authorities, with only 5 per cent harmonic distortion. GIM engineers are confident that this accuracy can be further improved to achieve an unprecedented 0.2 per cent. This means that the number of misrouted calls due to wide telephone systems tolerances will be greatly diminished if not entirely eliminated.
The ceramic crystal used with the MF telephone chip has been designed to GIM's specification, by Vernitron, Southampton. Ceramic crystals are an order of magnitude more stable than coil filters while being significantly cheaper than quartz crystals. Consequently the need to tune the MF circuit during manufacture is eliminated. Furthermore the elimination of the coil means that tone signals build up instantly.
Use of GIM's low power n-channel ion-implant process has reduced the power consumption of the AY-5-9400 to a mere 35 mW, or only 8 to 10 mA current drain, sufficient to supply the telephone directly from the line. An additional feature of the AY-5-9400 is a lock out circuit which inhibits the keyboard output when more than one key is pressed.
The basic AY-5-9400 is available in a 14 lead dual-in-line CERDIP package for conventional 10 key domestic telephones and a 16 pin version is also available for 16 key-pad data phones.
Both this circuit and the sister push-button dial microcircuit for use in Strowger networks can be paired with GIM's short number repertory dialler microcircuit. This MOS LSI microcircuit can store up to ten commonly used numbers, any one of which can subsequently be dialled with a single key depression.
This means that GIM can now supply push-button microcircuits to suit any telephone network in the world.



edwin amplifier

This is a design for a high-quality 40 W audio amplifier based on an earlier 20 W design which has proved very popular on the continent. The amplifier embodies some unusual design features and the construction is problem-free due to the small amount of negative feedback employed and to the absence of quiescent current in the output stage.

The Edwin amplifier is unusual in that it embodies two types of output stage in one amplifier. A class A output stage handles the low level signals and also serves as a driver for a class B stage which handles the larger outputs.

The principle of operation is shown in figure 1. T2 and T3 are biased on by the voltage drop across the diodes D1-D3. T2 and T3 function as a class A stage at low signal levels supplying current to the load via resistors R. As the signal is increased the voltage drop across these resistors becomes sufficient to cause T4 and T5 to conduct and the class B part of the output stage begins to operate. Crossover distortion is quite low with this type of design.

The complete circuit

As figure 2 shows, the complete amplifier circuit consists of a voltage amplifier, a class A driver stage and a class B output stage. The input stage consists of T1 and T2 in a Darlington configuration, resulting in a high input impedance. The signal passes to the base of T3 via the limiting resistor R4. T3 operates as a voltage amplifier and in its collector circuit has T4, which is connected as a simulated zener diode to provide a constant d.c. bias voltage of about 2 V across the bases of the driver transistors T7 and T8. Feedback is applied between the output and the junction of R11 and R12 to provide a high collector impedance so that true current drive is achieved. This helps to reduce crossover distortion still further so that despite the small amount of overall negative feedback and the absence of quiescent current in the output stage the distortion figures are very good.

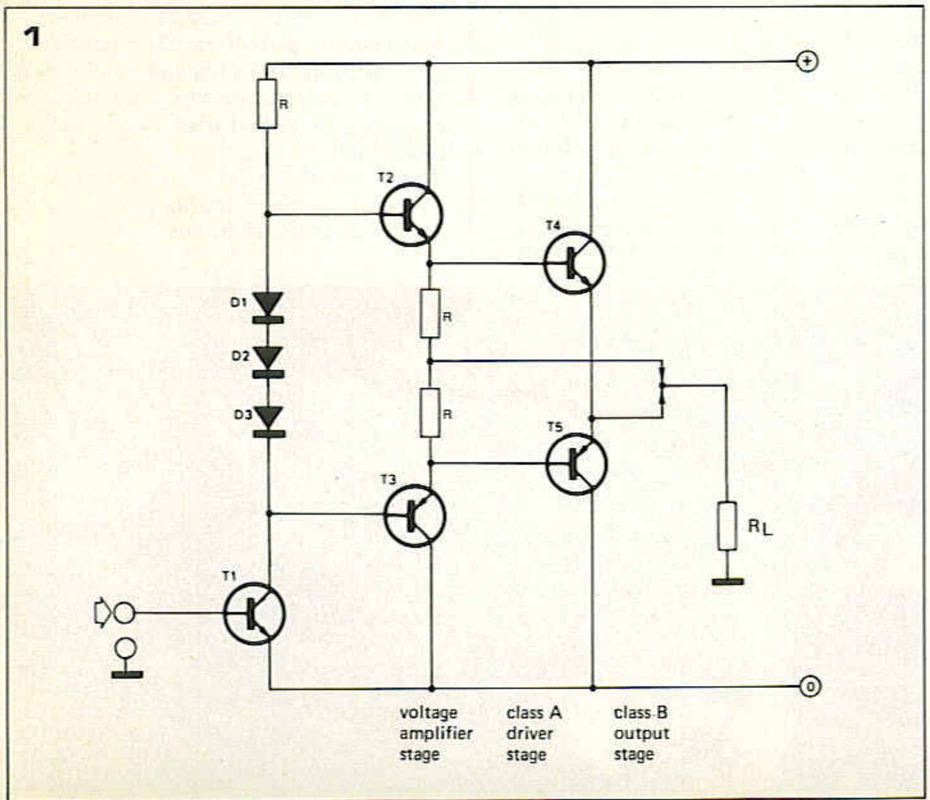
features

- output power from 10-40 W depending on power supply.
- high efficiency.
- low crossover distortion.
- short circuit proof.
- no quiescent current in the output transistors.
- output transistors and drivers need not be matched.
- unconditionally stable.

figures

- Sensitivity: ≈ 1 V (RMS).
- Input impedance: ≈ 45 kΩ.
- Distortion: 1 kHz, 30 W: 0.1%, 10 kHz, 30 W: 0.3%.
- Power bandwidth: 20 Hz – 100 kHz.
- S/N ratio: > 90 dB.

1



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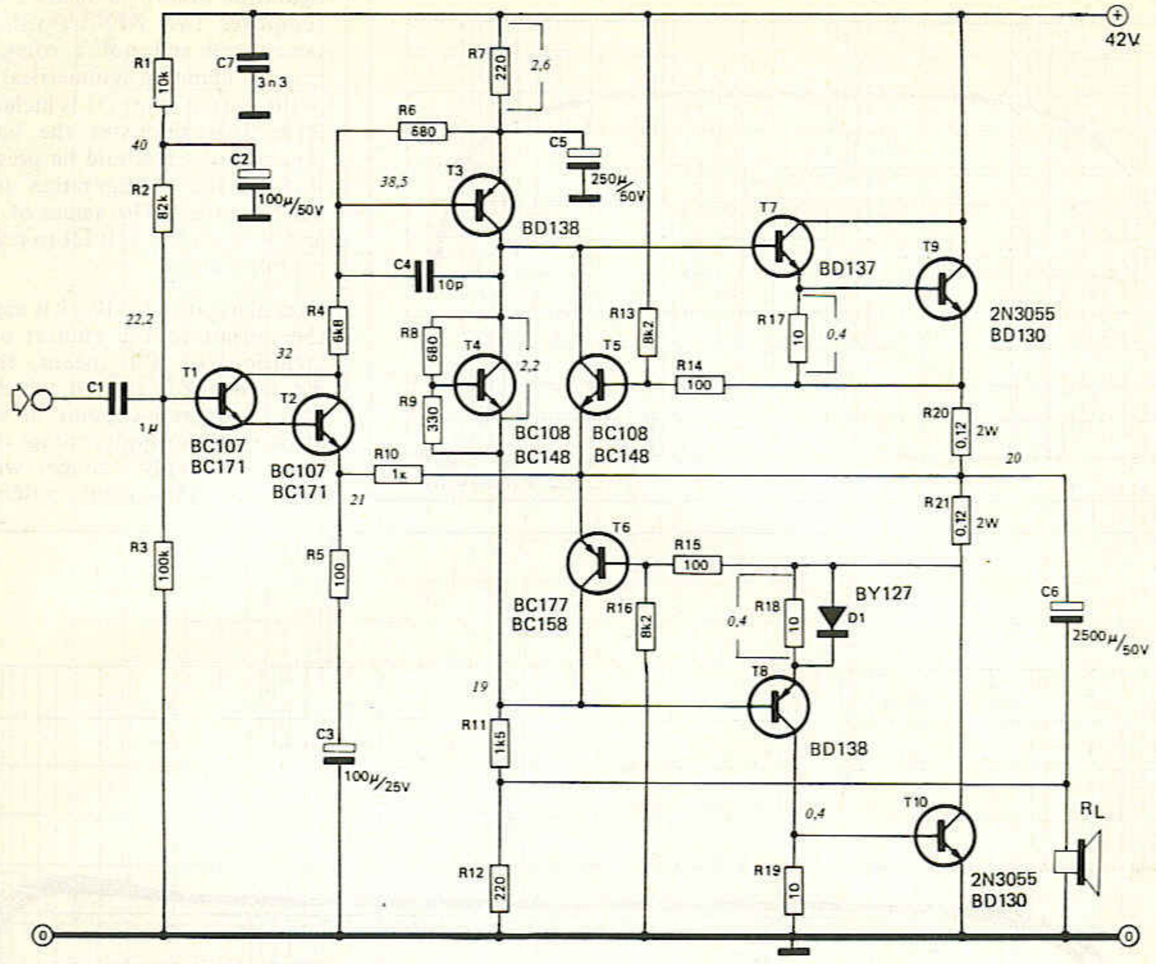

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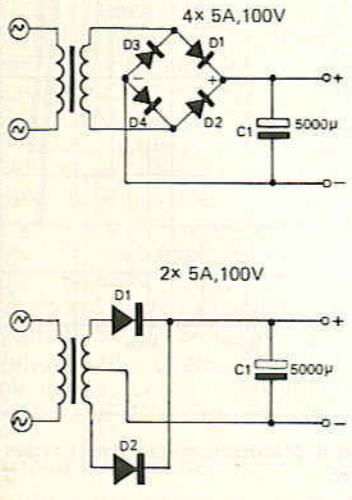

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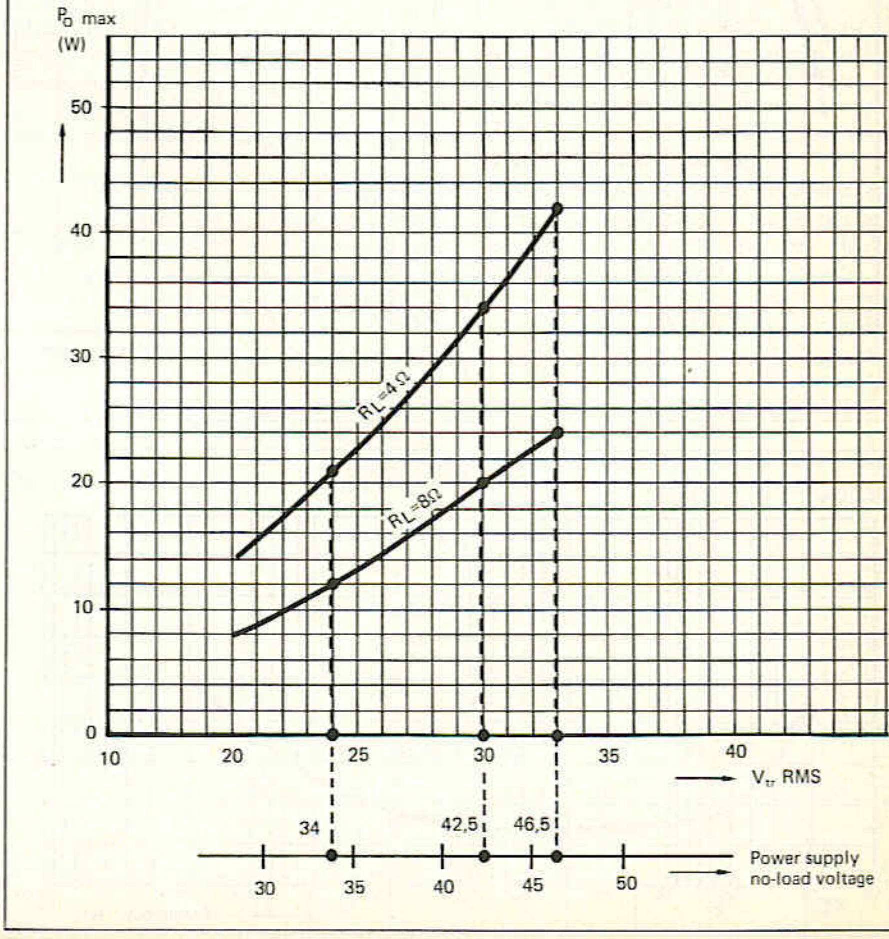
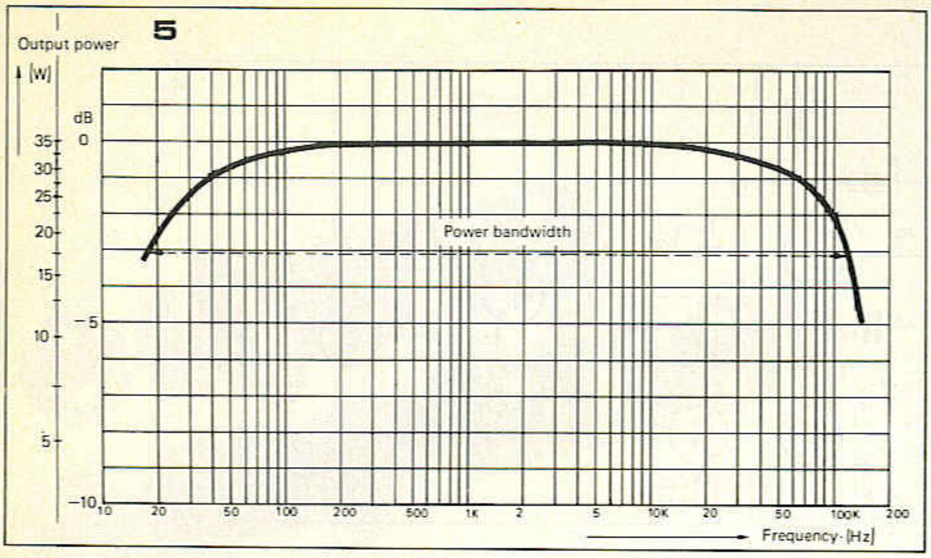


Figure 1. Basic circuit of an Edwin-type output stage.

Figure 2. Final circuit of the Edwin amplifier for output powers up to 40 W.

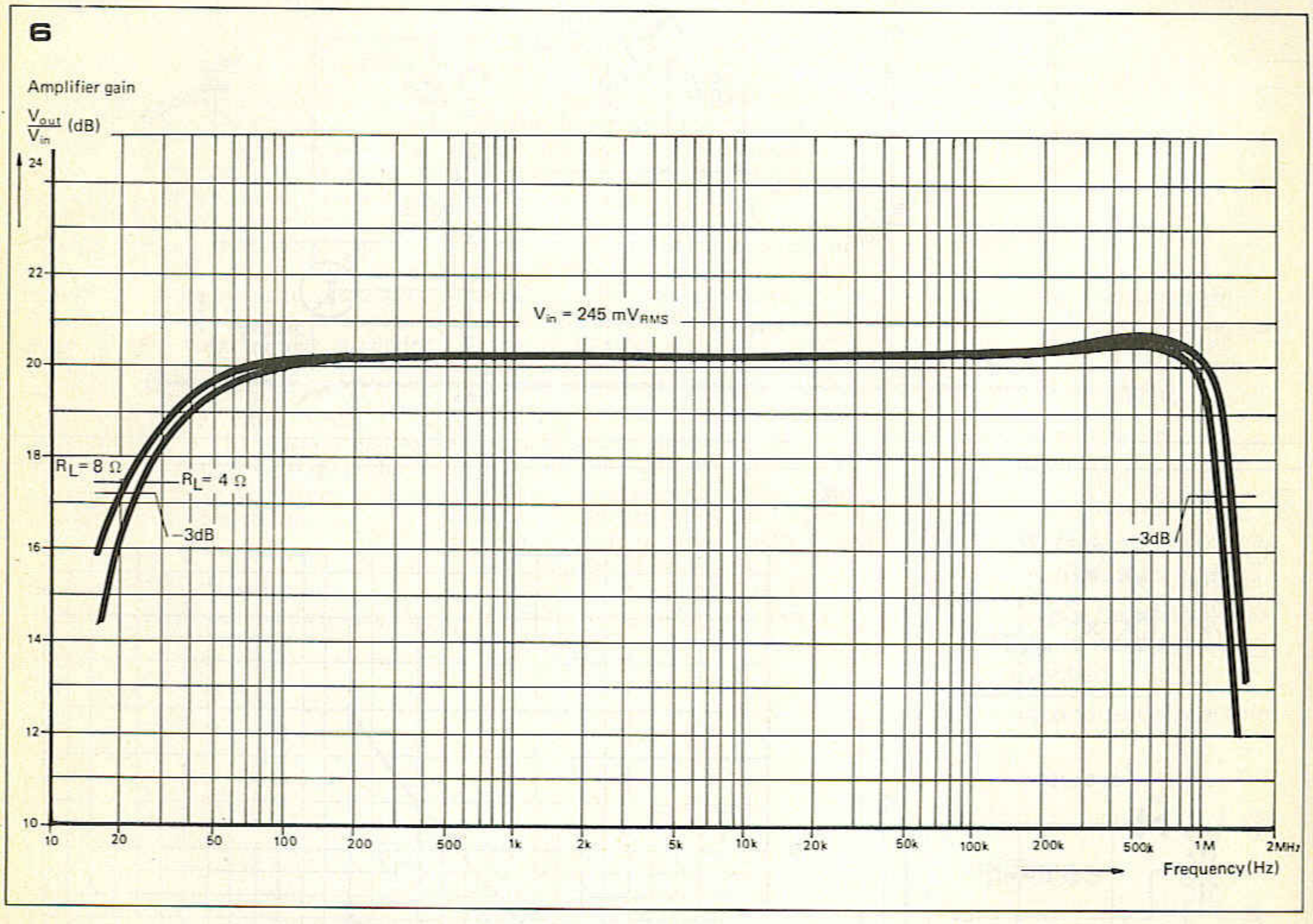
Figure 3. The power supply.

Figure 4. Graph of available output power versus transformer secondary voltage for 4 Ω and 8 Ω loads.



The output stage differs from the configuration shown in figure 1 because it comprises two NPN transistors of the same type and not a complementary pair. To maintain symmetrical operation of the output stage D1 is included across R18. This simulates the base-emitter junction which would be present across R18 if the configuration of figure 1 has been used. The values of R17, R18 and R19 are low (10 Ω) to reduce cross-over distortion.

Overall negative feedback is applied from the output to the emitter of T2. The inclusion of C3 means, that 100% d.c. feedback is applied, which stabilises the d.c. operating point of the output at around half supply voltage over a wide range of supply voltages without the need for adjustment potentiometers.



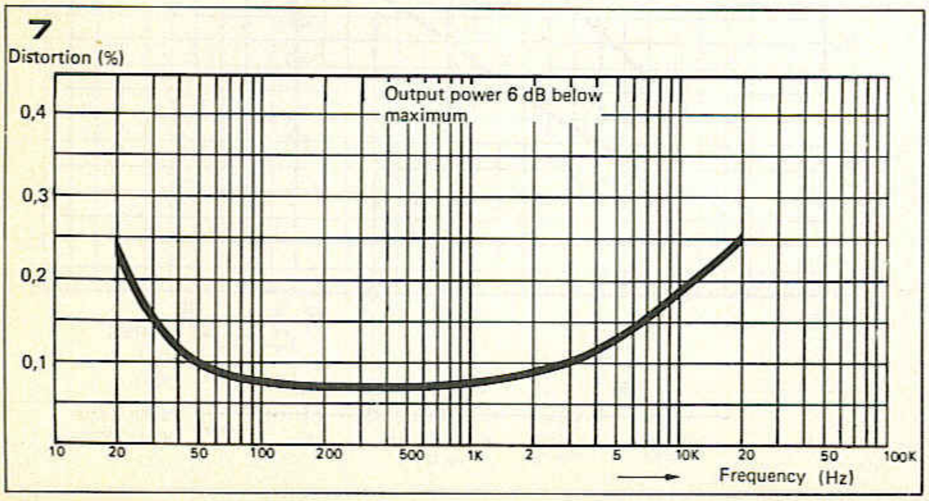


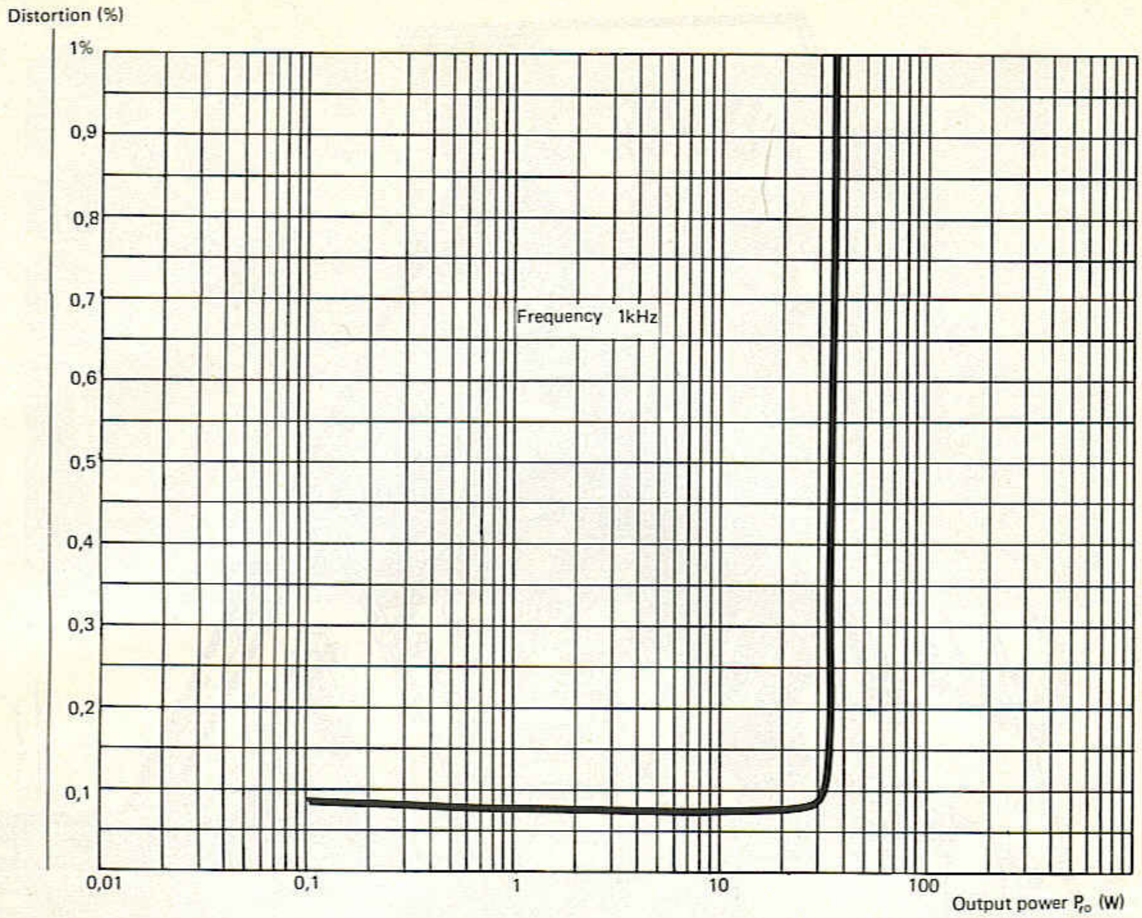
Figure 5. Maximum output power versus frequency.

Figure 6. Frequency response.

Figure 7. Distortion versus frequency for output power 6 dB below maximum.

Figure 8. Distortion versus output power.

8



The a.c. gain of the amplifier is, of course, given by

$$A_V = \frac{V_{out}}{V_{in}} = \frac{R_{10} + R_5}{R_5}.$$

It is worth noting the effect of the combination R7, C5 on the operation of the amplifier. Some amplifiers, when used with an unstabilised supply, display ripple on the peaks of the waveform when driven to clipping. This is eliminated by R7 and C5 as follows. When the amplifier is being driven, current flows through R7 and the voltage on C5 is always below the ripple 'troughs' on the supply. The drive voltage available from T3 is limited to the voltage on C5 and the output of the amplifier can never swing into the ripple region of the supply voltage. R7 also limits the current through T3 in the event of an overload.

Overload protection

The protection circuit is designed to prevent excessive current peaks from occurring during signal overloads or short-circuiting of the output. The protection circuit consists of transistors T5 and T6. Their base bias is set such that under normal operating conditions the voltage across R20 and R21 is insufficient to turn them on. In the event of excessive output current flowing in R20 or R21, due to a signal overload or a short-circuited output, the voltage across these resistors is sufficient to cause T5 or T6 to conduct. This reduces the drive voltage to the output stage and therefore limits the output current, thus protecting the amplifier.

Power supply

A stabilised power supply is unnecessary with the Edwin amplifier, as its performance will not be significantly improved. A simple unregulated supply is quite adequate and two suitable circuits are given in figure 3. Figure 3a shows a supply using a normal full-wave bridge rectifier, whilst figure 3b shows a full-wave rectifier with a centre-tapped transformer.

The component values and specification for supplies suitable for 20, 35 and 40 W versions of the amplifier are given in table 1. Of course any suitable transformer may be used, there is no need to adhere to the exact voltages specified. Figure 4 gives the output power available versus transformer secondary voltage. The only points to watch are that the current rating of the transformer is adequate for the required output power, that the voltage rating of the smoothing capacitor is sufficient and that the RMS secondary voltage of the transformer does not exceed 33 V on load, otherwise the voltage rating of the transistors may be exceeded.

Over the range of supply voltages given in figure 4 nothing need be changed in the amplifier as the operating point is self-adjusting.

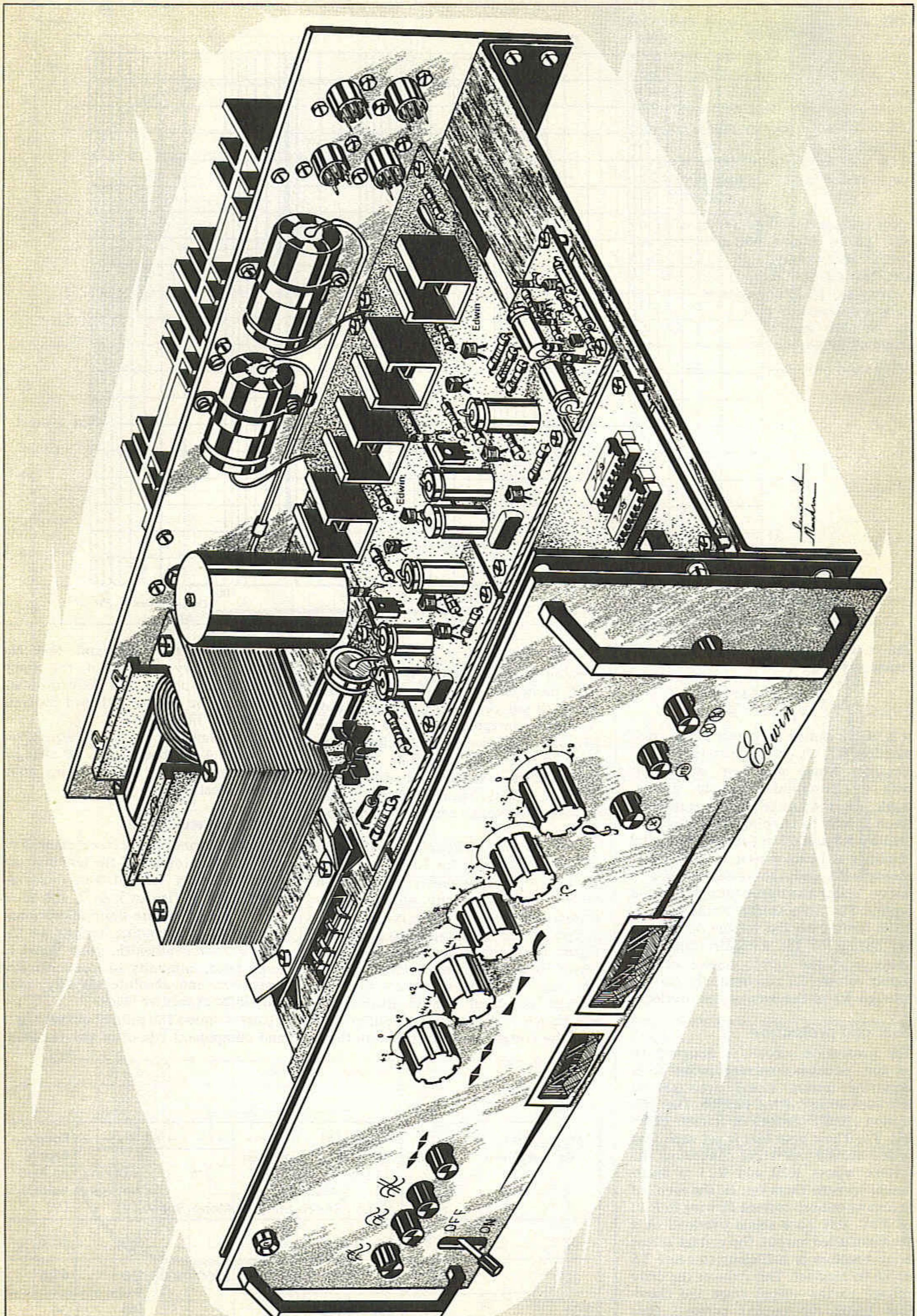
Performance figures

The performance figures, as measured on the 35 W prototype of the amplifier are summarised in table II and displayed graphically in figures 5, 6, 7, and 8. As can be seen they are quite exceptional. Among the outstanding features are the large power bandwidth, good signal to noise ratio, immunity to transients, low distortion and absolute stability, even with large capacitive loads.

Figure 9 shows the printed circuit board and component layout of the amplifier.

Table I

$P_{o\,max}$ (W) (R_L = 4 Ohm)	V_{tr} RMS	$I_{tr\,max}$ (A) figure 3b		figure 3a	C1 µF			Power supply no-load voltage (V)
		Mono	Mono Stereo	Stereo	Mono	Stereo	working voltage (V)	
42	33	1,1	2,2	4,5	2500	5000	60	46,5
35	30	1	2	4			50	42,5
21	24	0,8	1,5	3			40	34


Edwin
Edwin
Edwin
OFF
ON

9

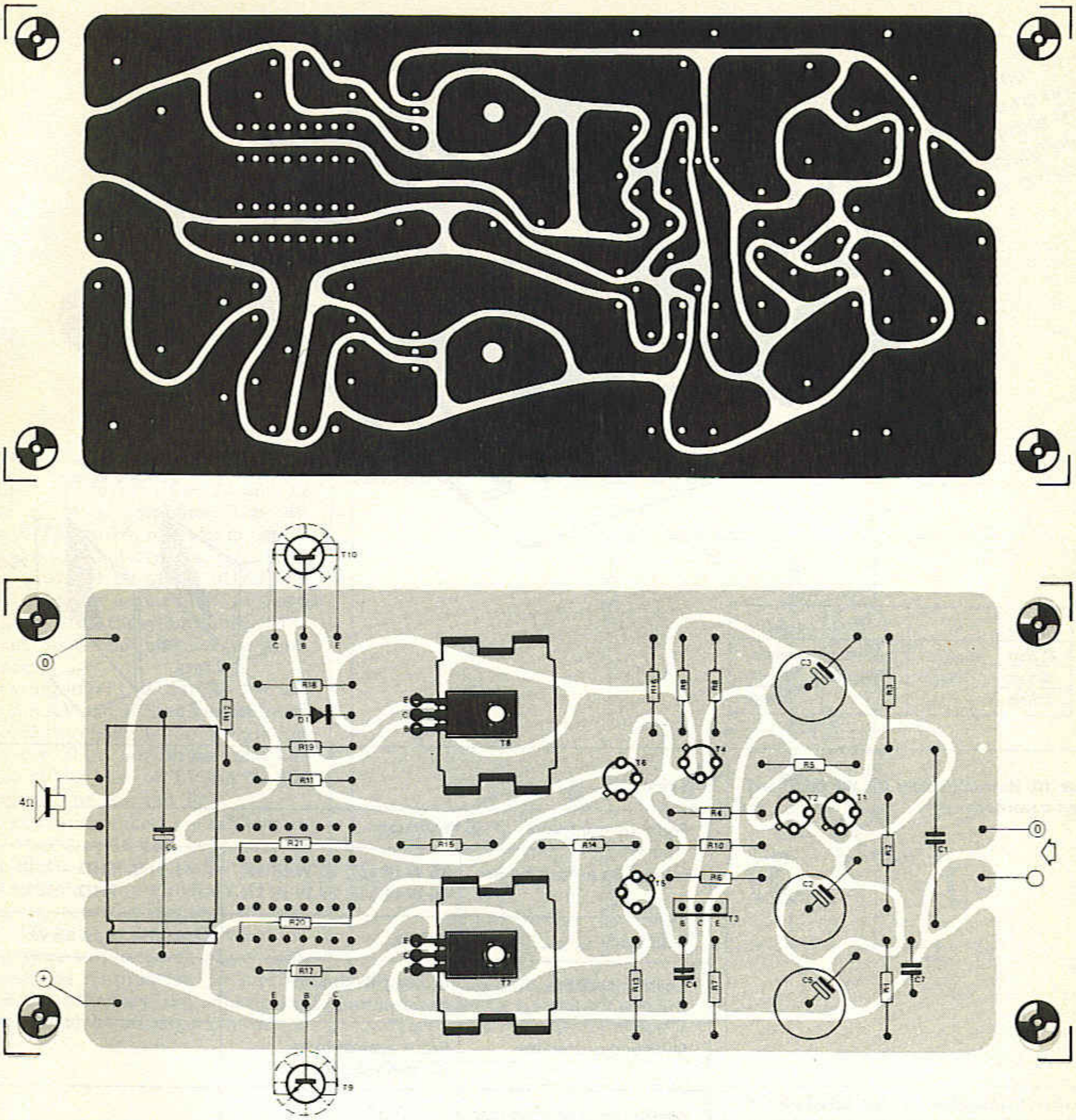


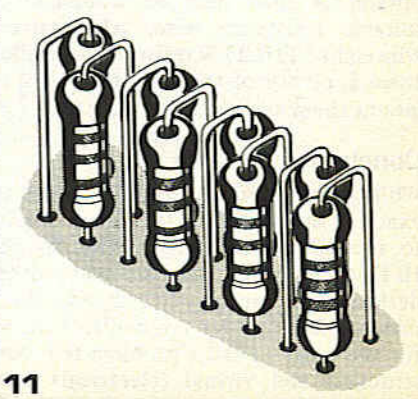
Figure 9. Printed circuit board and component layout.

Components list for figures 2 and 9

Resistors:
R1 = 10 k, ¼ W
R2 = 82 k, ¼ W
R3 = 100 k, ¼ W
R4 = 6k8, ¼ W
R5,R14,R15 = 100, ¼ W
R6,R8 = 680, ¼ W
R7,R12 = 220, ¼ W
R9 = 330, ¼ W
R10 = 1 k, ¼ W
R11 = 1k5, ¼ W
R13,R16 = 8k2, ¼ W
R17,R18,R19 = 10, ¼ W
R20,R21 = 0.12, 2 W

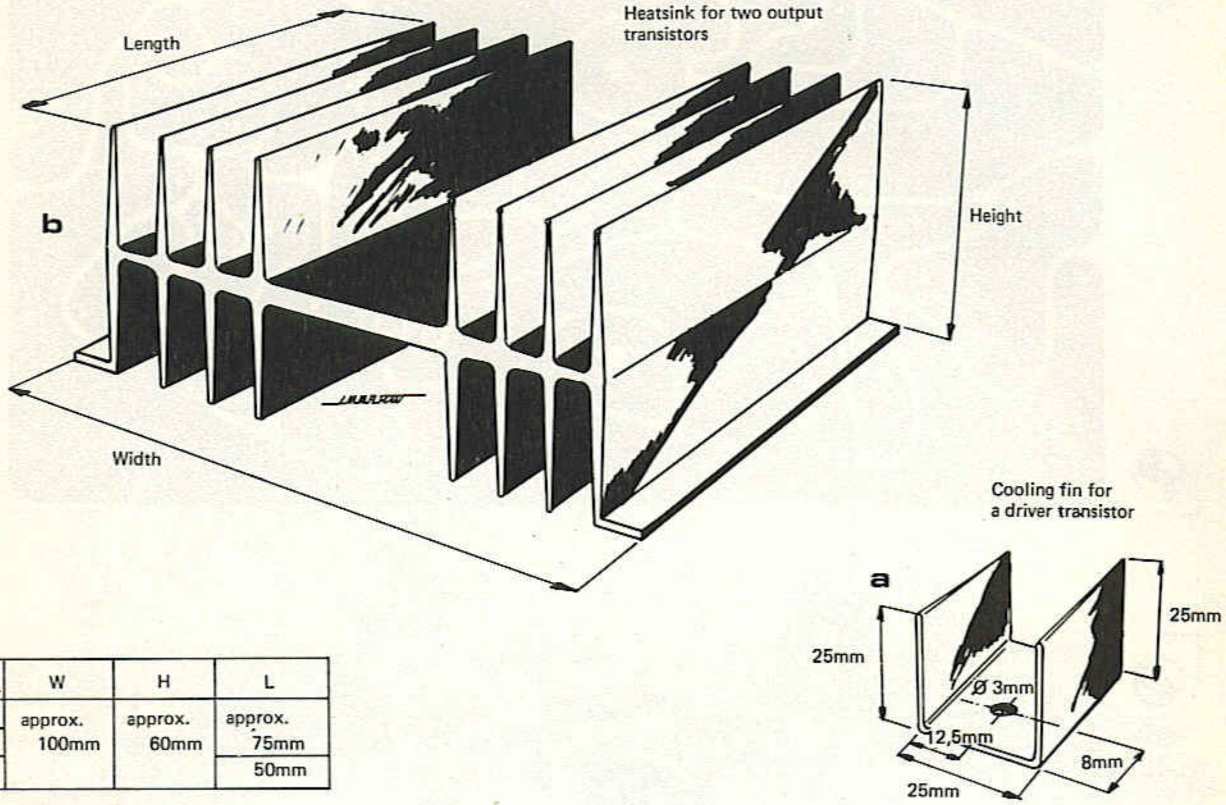
Capacitors:
C1 = 1 μ
C2 = 100 μ, 50 V
C3 = 100 μ, 25 V
C4 = 10 p ceramic
C5 = 250 μ, 50 V
C6 = 2500 μ, 50 V
C7 = 3n3

Semiconductors:
T1,T2 = BC 107, BC 171
T4,T5 = BC 108, BC 148
T3,T8 = BD 138
T6 = BC 178, BC 158
T7 = BD 137
T9,T10 = 2N3055, BD 130
D1 = BY 127



11

10


Length
Heatsink for two output transistors
b
Height
Width
Cooling fin for a driver transistor
a
25mm
25mm
Ø 3mm
12,5mm
8mm
25mm

P_o max.	W	H	L
42Watt	approx. 100mm	approx. 60mm	approx. 75mm
35Watt			
21Watt			50mm

Figure 10. Heatsink details for the driver and output transistors.

The driver transistors are mounted on the board, with a cooling fin as detailed in figure 10a. The output transistors are mounted on a separate extruded aluminium heatsink, details of which are given in figure 10b and the associated table. Most manufacturers of heatsinks will have something similar to this in their range.

If resistors R20 and R21 are not readily obtainable they may be wound from suitable resistance wire. Alternatively wire eight 1 Ω 0.25 W resistors in parallel, there is plenty of space on the board to mount them vertically (figure 11).

Concluding remarks

Whilst the Edwin amplifier meets an exacting specification this is no reason to recommend its construction by the Hi-Fi enthusiast. There are many other designs with similar performance. What makes the amplifier eminently suitable for the amateur is its problem-free construction and virtual (electrical) indestructibility. ◀

Table II

Performance figures of 35 W version		
Maximum output power	35 W (4 Ω); 20 W (8 Ω) 45 W (4 Ω); 27 W (8 Ω)	f = 1 kHz, THD = 1 % THD = 10%
Efficiency	>60%	f = 1 kHz; P_o = 35 W
Load impedance	0 ... ∞ (Maximum power into 4 Ω)	
Overload protection	Proof against long duration short-circuit	
Maximum capacitive load	>100 µF (!)	
Sensitivity	≈1 V RMS	f = 1 kHz, P_o = 35 W
Input impedance	≈45 kΩ	
Distortion		P_o = 0 ... 30 W
	0,1%	f = 1 kHz
	0,2%	f = 30 Hz
	0,3%	f = 10 kHz
Frequency response	25 Hz ... 1,2 MHz (−3 dB) 40 Hz ... 1,0 MHz (−1 dB)	V_{in} = 245 mV
Power bandwidth	>100 kHz (−3 dB)	
Noise rejection	73 dB 93 dB	input open-circuit input short-circuit
Signal to noise ratio	95 dB >105 dB	input open-circuit input short-circuit
Feedback factor	≈36 dB	
Stability	unconditional	

miniature amplifier

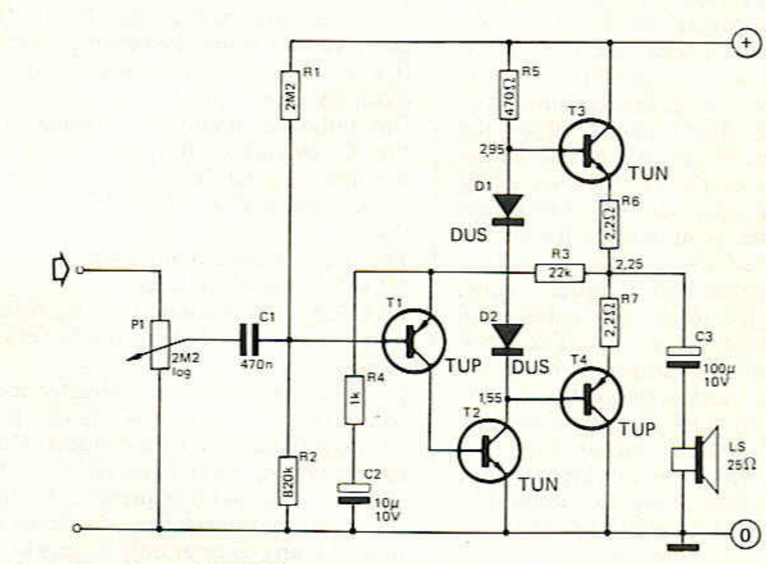
For the younger constructor with limited funds it is necessary to be very cost-conscious when designing circuits. This circuit for a simple record player amplifier fulfils these requirements. The circuit will operate from a 4.5 V battery and can be used to amplify the output of a crystal pickup to drive a small loudspeaker or headphones. The circuit is not outstanding for its power or quality, but it is simple and reliable.

The input and driver stages T1 and T2 operate as voltage amplifiers. The output stage, T3 and T4, operates in class B to achieve long battery life. D.C. feedback is provided by means of R3 and A.C. feedback by means of R3, R4 and C2. This defines the gain, stabilises the operating point and increases the input impedance.

The biassing of T1 is critical and the values for R1 and R2 must be adhered to. Should the circuit fail to operate correctly the D.C. conditions may be checked at the base of T3 and T4 and the junction of R6 and R7.

If 25 ohm loudspeakers are difficult to obtain, then 8 or 15 ohm types may be used instead. In that case R6 and R7 should be replaced by wire links.

As can be seen from figure 2 the p.c. board is extremely miniature and finding space in the record player cabinet should be no problem. To improve loudspeaker efficiency the loudspeaker cabinet should be as large as possible.



Input impedance $Z_1 \geq 600$ k
Input sensitivity v_i = 200 mV (r.m.s.)
Output power (with 25 Ω) P = 50 mW.

Parts list.

Resistors:
R1 = 2M2
R2 = 820 k
R9 = 22 k
R4 = 1 k
R5 = 470 Ω
R6 = 2.2 Ω
R7 = 2.2 Ω
P1 = 2M2 log

Capacitors:
C1 = 470 n
C2 = 10 µ/10 V
C3 = 100 µ/10 V

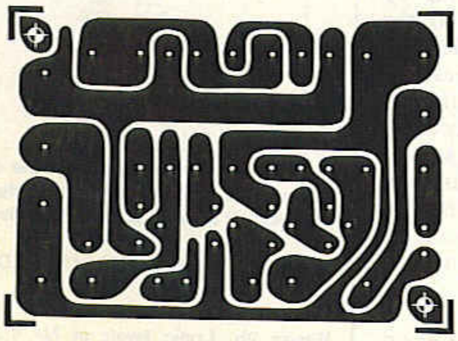
Semiconductors:
T1,T4 = TUP
T2,T3 = TUN
D1,D2 = DUS

Sundries:
Torch battery 4.5 V
Loudspeaker 25 Ω

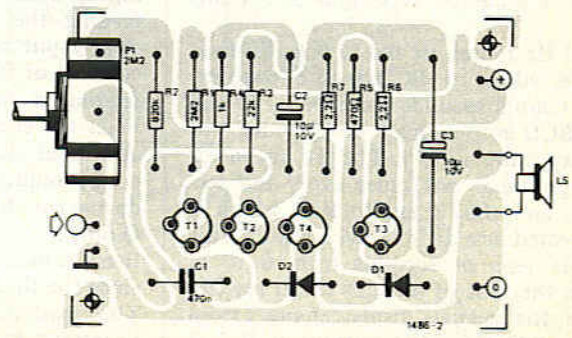
Figure 1. The very simple amplifier circuit.

Figure 2. Layout of match-box size printed-circuit board.

1



2



versatile digital clock

'One-chip' digital clocks, such as the MM5314 (Elektor 1, p. 24), are excellent for simple time-keeping. However, they are not ideal for driving external devices such as time signals, calendars, etc. This is where a 'conventional' clock design with standard TTL ICs scores; it has a BCD-coded time output, as well as pulse train outputs giving repetition rates varying from one per second to one per day. Several external devices for use with the clock described here will be published in future issues of Elektor.

Elektor has previously published designs for 'one-chip' digital clocks, with both mains and crystal reference frequencies. Whilst ICs such as the MM5314 are excellent for simple timekeeping, they have certain disadvantages. Since the output to the display is multiplexed the time output of the clock is not easily accessible in a parallel form. This means that the clock is unsuitable for driving time-controlled devices such as alarms, calendars, central heating programming, automatic recording of radio programmes or other systems. The clock described in this article is based on TTL circuitry and is eminently suitable for control systems. The time is available as a BCD coded output, and clock pulse trains with rates varying from one a second to one a day are obtainable. Many constructors will probably have some of the ICs in their 'junk box'.

The complete circuit of the clock (excluding power supply) is given in figure 1. The basic operation is quite simple. With all the switches in the positions shown the clock runs normally. The 50 Hz input is rectified by D1, clamped to 4.7 V by D2 and then fed into the NAND Schmitt trigger ST1. A 50 Hz square wave suitable for driving TTL appears at the output of ST1 and is fed to IC10 which is connected as a divide-by-five counter. Asymmetric 10 Hz pulses are available at the 'D' output of IC10. These pulses are fed to IC9, which is connected as a divide-by-10 counter. A symmetrical 1 Hz square wave is available at output 'A' of this IC.

The 1 Hz pulses are fed to IC6, which is connected as a BCD decade counter. This counts seconds from 0 to 10 and the BCD output may be decoded for display using a 7447. The 'D' output of IC6 produces one pulse every ten seconds, and this is fed to IC5, which is connected as a divide-by-6 counter. This counts tens of seconds from 0 to 6. When the tens of seconds count reaches 6 (i.e. the seconds display changes from 59 to 60) the BCD output of IC5 is 0110, that is to say the 'B' and 'C' outputs of the IC are both '1'. These outputs are connected to the Reset 0 inputs, so that when the count reaches 6 IC5 is reset instantaneously, and the 6 display is never seen.

One pulse per minute is obtained from the 'C' output of IC5, and this is fed through N2 and N1 to IC4, which is again connected as a BCD decade counter.

The time-setting circuits around N1 and N2 will be discussed later.

Like IC5, IC3 is connected as a divide-by-6 counter, so that it counts tens of minutes.

Counting of the hours is slightly more complicated. Since the clock is a 24 hour design, the hours counter (IC2) must count up to 10 twice, then reset at 4 on the third count sequence (i.e. when the hours count reaches 24). Since the tens of hours counter only counts to 2 a counter is made up from two JK flipflops (7473) instead of using a 7490. Resetting is accomplished as follows: During the first 0-10 count of IC2 the Q outputs of FF1 and FF2 are low. When the 'D' output of IC2 goes low on the tenth count the Q output of FF1 goes high. At the end of the second count sequence the Q output of FF1 goes low and the Q output of FF2 goes high. The Q output of FF2 and the 'C' output of IC2 are connected to the Reset 0 inputs of IC2, so that when IC2 reaches 4 in its third count sequence it is reset. However FF2 cannot similarly be reset as it has no gating on the clear input. This difficulty is overcome by feeding the 'B' output of IC2 to the clear input of FF2 via C1 and R3. On count 4 of IC2 the 'B' output goes low, feeding a momentary reset pulse to FF2. Of course this occurs at count 8 also, and during the first and second count sequences. However, it is only during the third count sequence that the Q output of FF1 is high anyway, so these earlier reset pulses do not matter, since the flipflop is reset already.

The capacitive coupling (C1, R3) is necessary to ensure that only a short reset pulse is provided. If direct coupling were used then the clear input would be held low on count 10 during the second count sequence, and the Q output of FF2 could not go high.

Provision of 'tick'

It will be noted that IC9 is connected differently from the other divide-by-10 counters (IC2, IC4 and IC6). This is because a BCD output is required from the other counters. IC9 is connected to give a symmetrical square-wave output, as a convenient simulated 'tick', and this happens to sound better with a 1:1 mark-space ratio.

Time-setting

Three time-setting switches are provided. Two to make the clock advance at a fast rate, and one to stop the clock. This is useful because the clock can be set to a particular time, stopped, then the stop button can be released exactly on the time signal from radio or telephone. It is also handy if the clock is accidentally advanced too far as it saves going all the way 'round the dial'. Gating for the time-setting is provided by a 7400 (IC7) plus the spare half of the 7413 Schmitt trigger (½IC8).

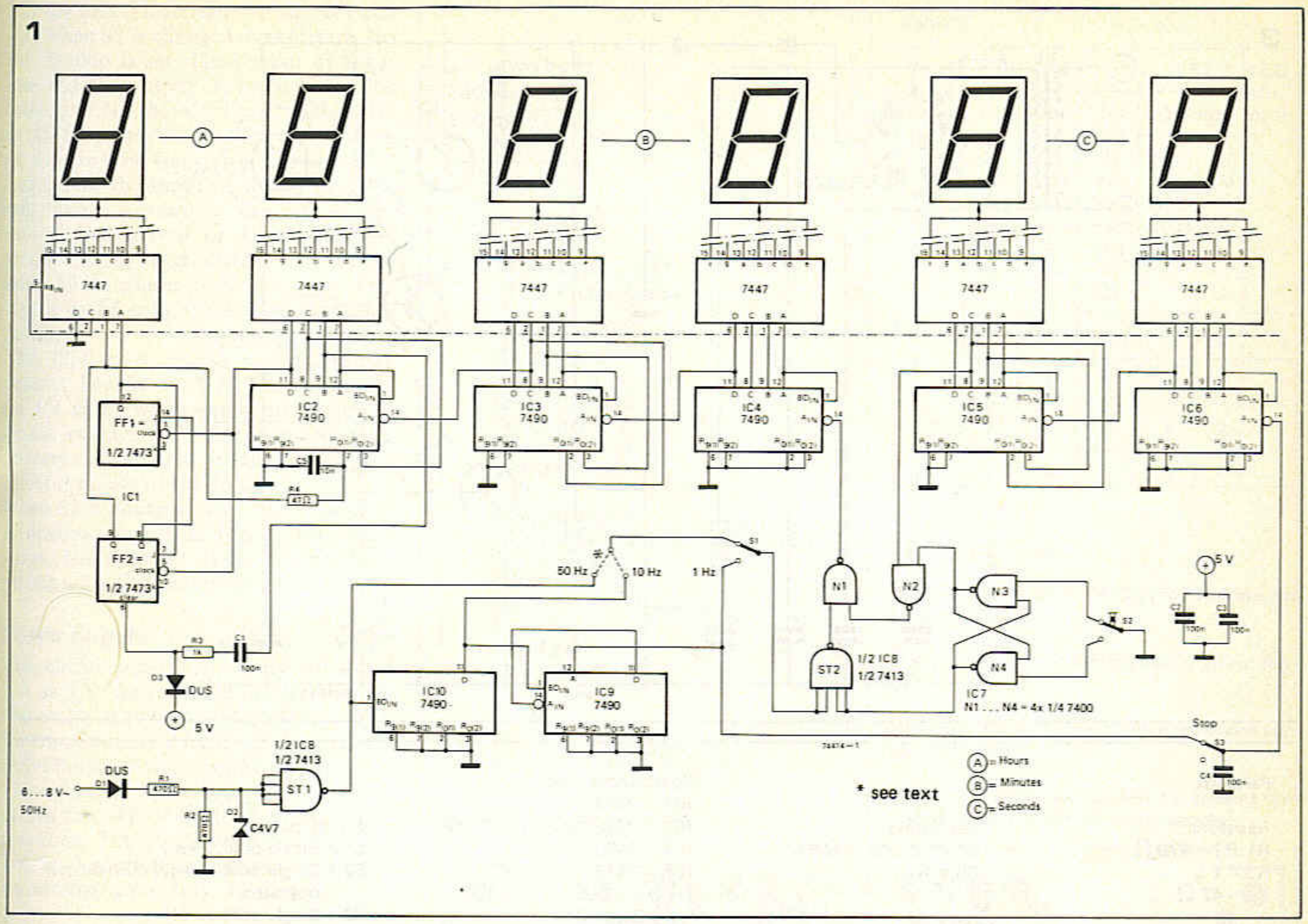
The operation is as follows: when S2 is in the position shown in figure 2a the set-reset flipflop N3/N4 is reset, so the output of N3 is high and the output of N4 is low. This means that the output of ST2 is high. Pulses from output 'C' of

Figure 1. Circuit diagram of the clock. The printed circuit board does not include the display and its associated decoder/drivers.

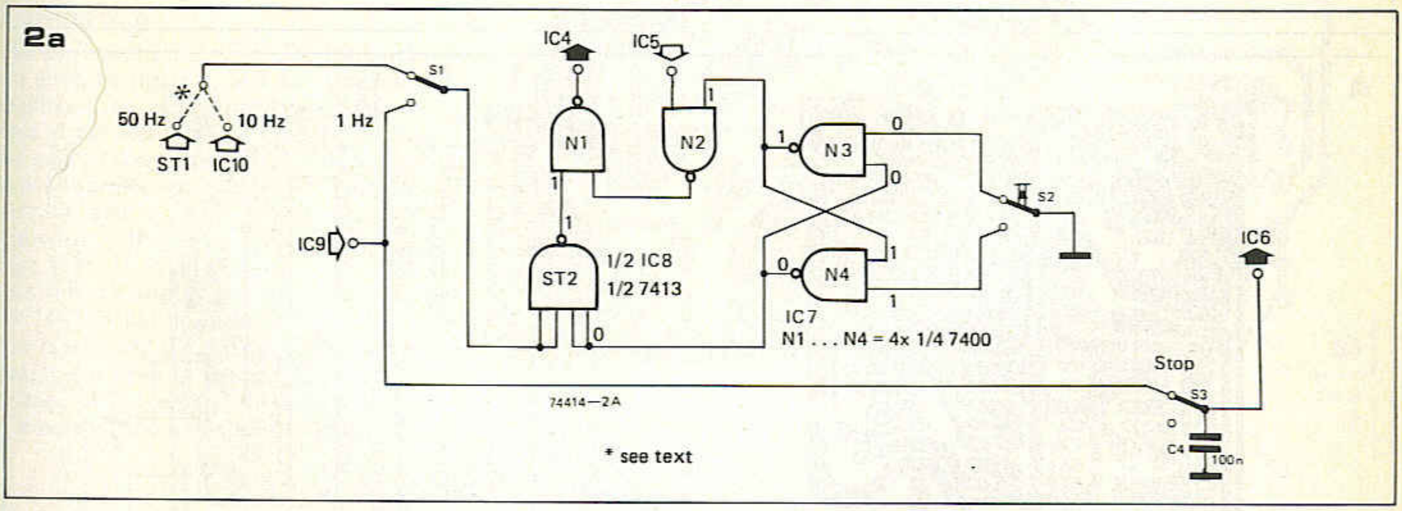
Figure 2a. Logic levels at NAND gates for normal timekeeping.

Figure 2b. Logic levels at NAND gates for time-setting.

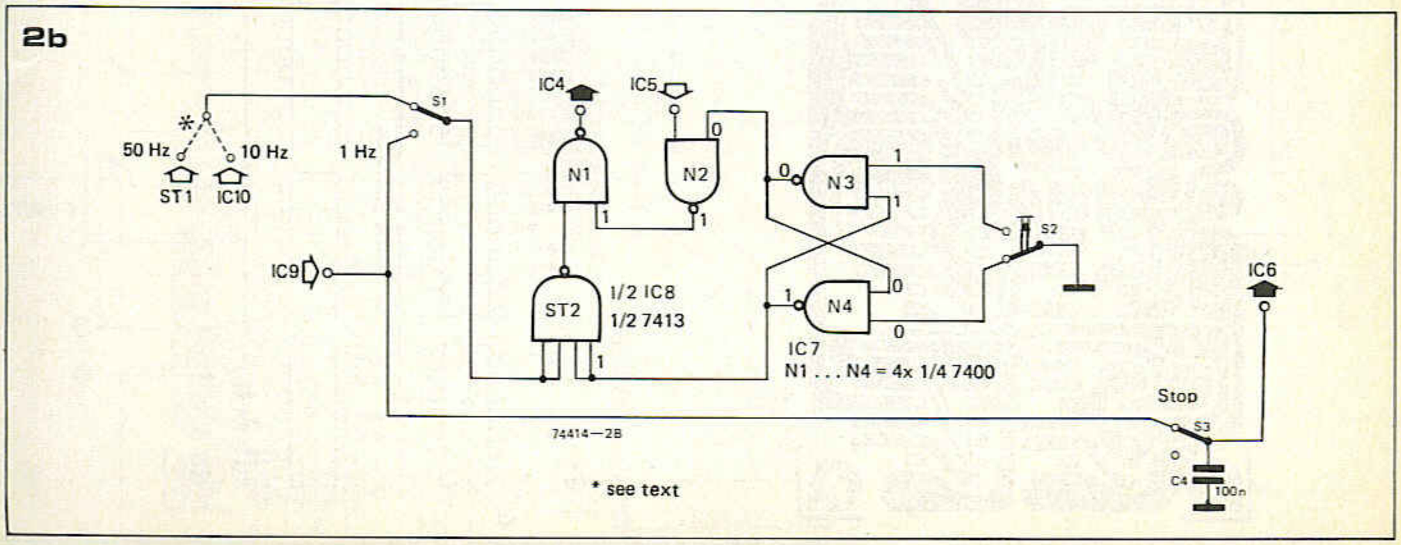
1


A
B
C
7447
IC2 7490
IC3 7490
IC4 7490
IC5 7490
IC6 7490
FF1 = 1/2 7473
FF2 = 1/2 7473
IC1
C5 10n
R4 47Ω
R3 1k
C1 100n
D3 DUS
5 V
50 Hz
10 Hz
1 Hz
S1
N1
N2
N3
N4
S2
ST2
1/2 IC8 1/2 7413
IC7
N1 . . . N4 = 4x 1/4 7400
IC10 7490
IC9 7490
1/2 IC8 1/2 7413
ST1
6 . . . 8 V~ 50Hz
D1 DUS
R1 470Ω
R2 470Ω
D2 C4V7
+5 V
C2 100n
C3 100n
Stop
S3
C4 100n
74414—1
* see text
A = Hours
B = Minutes
C = Seconds

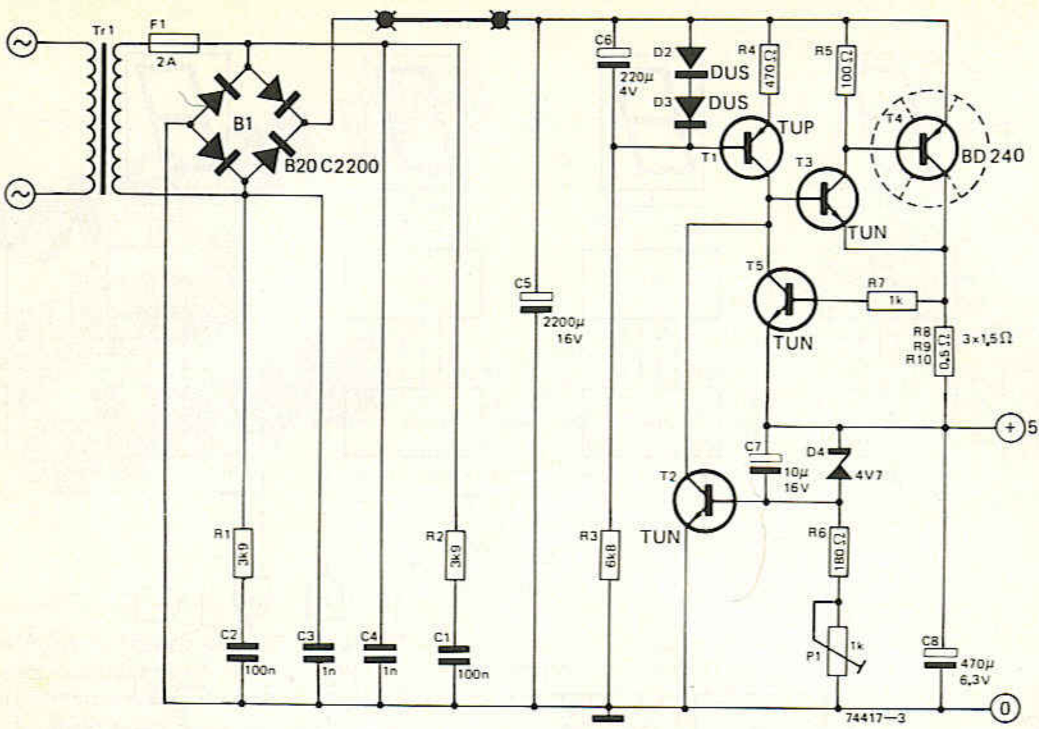
2a


*
50 Hz
10 Hz
ST1
IC10
S1
1 Hz
IC4
IC5
N1
N2
N3
N4
1
0
IC9
ST2
1/2 IC8
1/2 7413
S2
IC6
IC7
N1 . . . N4 = 4x 1/4 7400
Stop
S3
C4
100n
74414—2A
* see text

2b


*
50 Hz
10 Hz
ST1
IC10
S1
1 Hz
IC4
IC5
N1
N2
N3
N4
1
0
IC9
ST2
1/2 IC8
1/2 7413
S2
IC6
IC7
N1 . . . N4 = 4x 1/4 7400
Stop
S3
C4
100n
74414—2B
* see text

3



Parts list

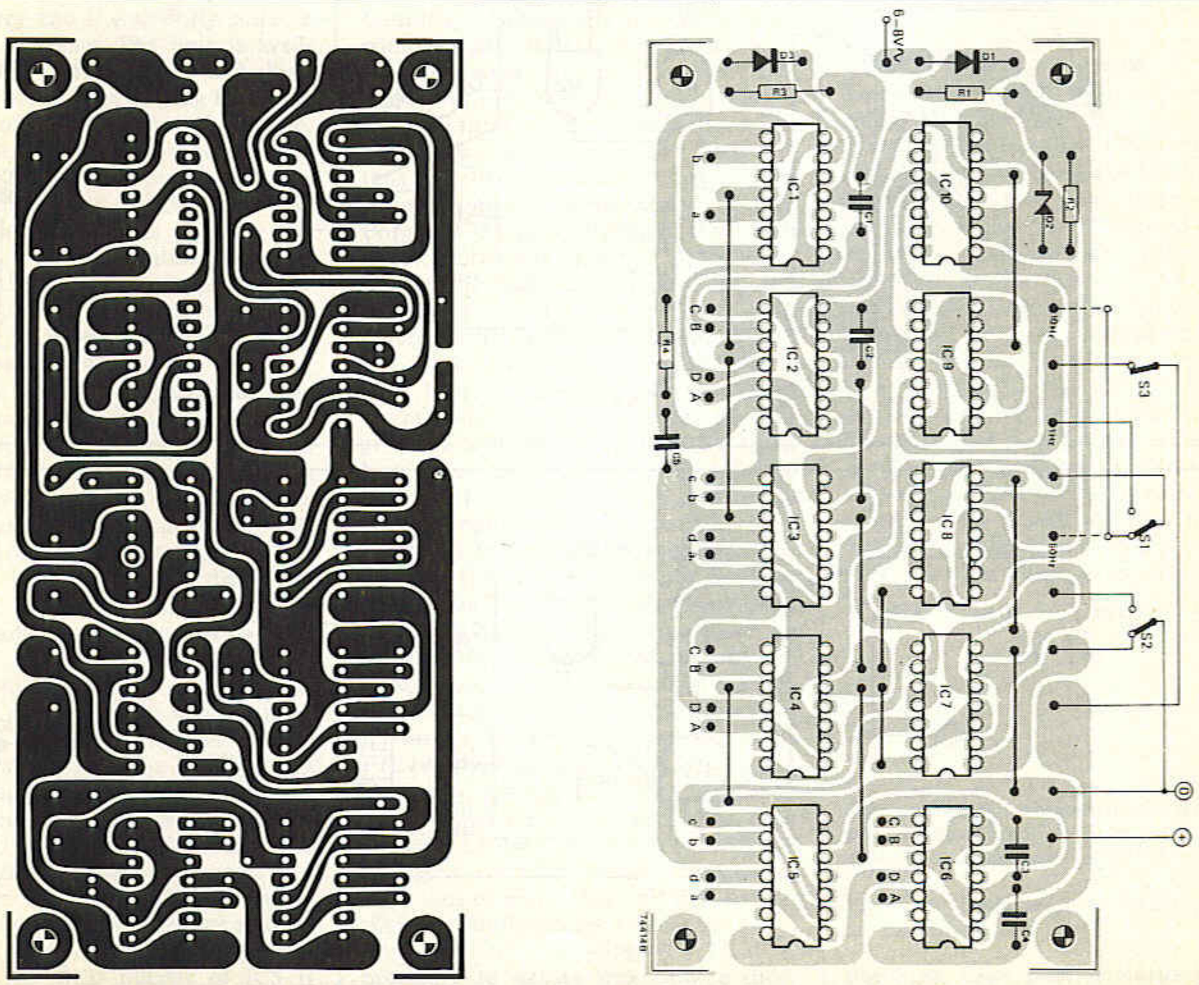
Resistors:
R1,R2 = 470 Ω
R3 = 1 k
R4 = 47 Ω

Capacitors:
C1,C2,C3,C4 = 100 n
C5 = 10 n

Semiconductors:
IC1 = 7473
IC2 ... IC6,IC9,IC10 = 7490
IC7 = 7400
IC8 = 7413
D1,D3 = DUS
D2 = Zener C4V7

Switches:
S1 = Single-pole, 2-way
S2 = Single-pole, 2-way, push-button operated
S3 = Single-pole on-off

4



IC5 are thus transferred through N2 and N1. When S2 is changed over (figure 2b) the flipflop is set. The output of N3 is low and the output of N4 is high. The output of N2 therefore goes high. 1 Hz or 10 Hz pulses (depending on position of S1) are now transferred through ST2 and N1 to the input of IC4. The clock will therefore count at the rate of one minute per second or 10 minutes per second. As an alternative to the 10 Hz rate, 50 Hz pulses may be used. This rate is useful only for setting the hours rapidly.

The flipflop is necessary to suppress contact bounce on S2. The flipflop is set (or reset) when the switch initially makes contact on being changed over. Subsequent switch bounce will not affect the state of the flipflop.

When S3 is changed over the 1 Hz drive is disconnected from IC6 so the clock stops. The position of S3 during time-setting with S2 is unimportant.

Power Supply

The clock requires a supply of about 1 A at 5 V. As transient interference on the mains supply could interfere with the timekeeping of the clock a stable, well-filtered mains supply is essential. The circuit of figure 3 is recommended, as this can deliver up to 2 A and is well stabilised. The 50 Hz drive for the clock can be derived from either side of the transformer secondary winding.

Construction

The p.c. board and layout for the clock are given in figure 4, and the assembly requires little comment. The BCD outputs of the counters are brought out to the edge of the board. Display decoding is not provided on the board. Suitable decoder and display boards are the 'Universal Display' (Elektor No 2, Page 223). If zero suppression on the tens of hours display is required pin 5 of the 7447 should be grounded.

The layout and p.c. board of the power supply are given in figure 5. The output voltage of the supply should be set to 5 V before connecting to the clock.

Table 1

COUNT	INPUTS D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Parts list

Resistors:
R1,R2 = 3k9
R3 = 6k8
R4 = 470 Ω
R5 = 100 Ω
R6 = 180 Ω
R7 = 1 k
R8,R9,R10 = 1.5 Ω
P1 = 1 k, preset

Capacitors:
C1,C2 = 100 n
C3,C4 = 1 n
C5 = 2200 µ/16 V
C6 = 220 µ/4 V
C7 = 10 µ/16 V
C8 = 470 µ/6.3 V

Semiconductors:
B1 = Bridge rectifier, e.g. B20C2200
D1 = omitted
D2,D3 = DUS
D4 = zener 4.7 V, 400 mW
T1 = TUP
T2,T3,T5 = TUN
T4 = BD240 or equ.

Sundries:
F1 = 2 A delay-action fuse
Tr1 = transformer, 8 V/2 A

Table 2

Clock Pulse Number	FF1 In-put J1 (14) con-nected to $\overline{Q}2$	FF1 Out-put Q1 (12) BCD Code A	FF2 In-put J2 (7) con-nected to Q1	FF2 Outputs Q2 (9) BCD Code B	FF2 Outputs $\overline{Q}2$ (8)	LED dis-play
	1	0	0	0	1	0
1	1	1	1	0	1	1
2	0	0	0	1	0	2
3	1	0	0	0	1	0

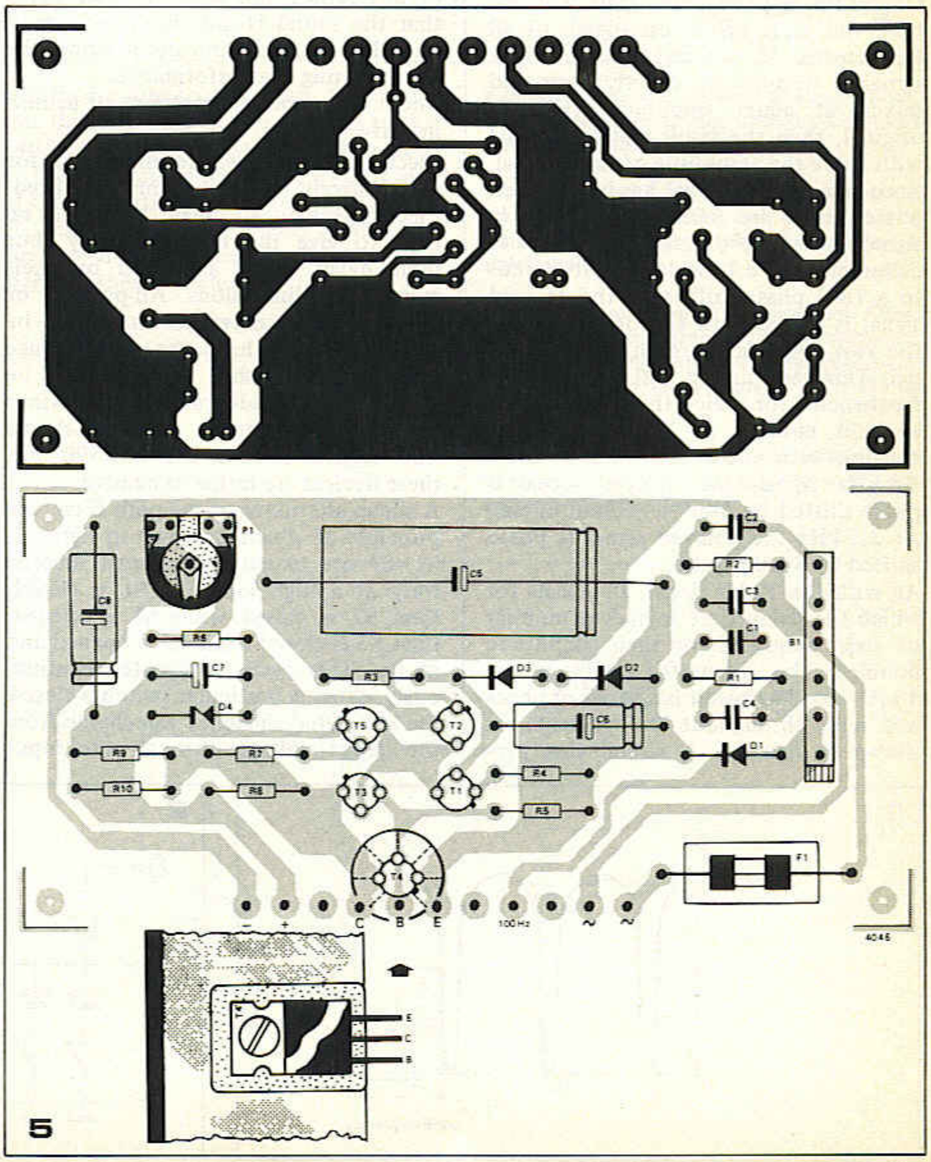
Table 1. BCD code.

Table 2. Truth table for IC1 (7473 connected as 1:3 divider).

Figure 3. Circuit of 5-V stabilised power supply.

Figure 4. Printed circuit and component layout of the clock.

Figure 5. Printed circuit and component layout of the 5-V stabilised power supply.



5

G. Knapienski and F. Mitschke

phasing

Nowadays there are a great number of methods of producing unusual electronic sound effects. A favourite effect is 'Phasing' and in this article this is accomplished, somewhat unusually, by using a 'path filter'. This is a cheap alternative to the already well-known, charge-coupled analogue shift register or 'bucket brigade' memory.

Phasing occurs when a portion of a signal is delayed and then mixed with the original signal. In the middle of the audio spectrum delays of less than about 100 μs will produce no noticeable effect, whilst delays greater than about 30 ms will produce a distinct echo. A delay between these limits will give the required 'phasing' effect.

Of course, a fixed delay time will not have the same effect on signals of all frequencies. If, for example, a 1 kHz signal is delayed by exactly 1 ms and mixed at equal amplitude with the original, then the result will be a signal with twice the amplitude of the original, since the delayed signal has in fact been phase-shifted by 360°. For a 500 Hz signal, however, the situation is quite different. Here a 1 ms delay corresponds to a 180° phase shift, so if the delayed signal is mixed with the original signal the two will cancel, resulting in no signal. This cancellation will occur for all frequencies for which the delay time is an odd number of half-periods. For example with a delay time of 1 ms and a 1.5 kHz signal, the delayed signal is phase shifted by 540°, or 3 half cycles. At 2.5 kHz the delayed signal is phase shifted by 5 half-cycles.

As with the 1 kHz signal, all signals for which the delay time is an even number of half periods have their amplitude doubled. This is true for 2 kHz, 3 kHz, 4 kHz etc. The result is a series of peaks and nulls throughout the spectrum, as shown in figure 1. A circuit that produces this type of response is known as a 'comb filter', because of the unusual shape of the response curve.

Practical Realisation

Early attempts at phasing often used tape recorders running slightly out of synchronism, but this entails a number of difficulties, not least of which being that the sound is not 'live', and consequently the musician cannot adjust the sound during the performance.

There are numerous methods of achieving 'live' phasing.

Electrical delay lines are impractical for the relatively long delay times required. Electromechanical delay lines can be used to give the required delay, but their delay times are fixed by their mechanical dimensions. All-pass LC or RC phase-shift networks may also be used, but these have the disadvantage that the phase shift cannot easily be varied over a wide range. An obvious solution would be to use an analogue shift register such as the TCA590, but these devices are rather expensive.

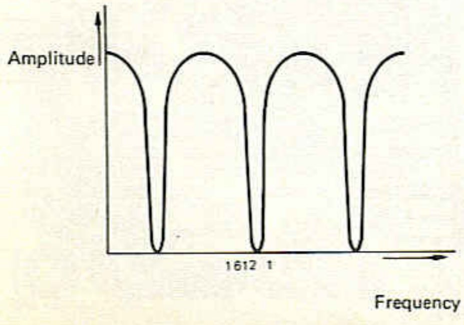
A cheap alternative is the path filter, the principle of which is shown in figure 2. S1–S7 are closed and opened successively at a high rate, i.e. S1 is closed, then S2 is closed while S1 is opened, then S3 is closed while S2 is opened and so on. This cycle is repeated continuously. When a particular switch is closed, the associated capacitor can charge from the input voltage through the input resistor R. The voltage on each capacitor is dependent on the time constant RC (which is fixed if all the capacitors have the same value) the time for which each switch remains closed (which is also fixed) and the instantaneous level of the input signal.

It is therefore apparent that after a cycle of the switch sequence the voltages on the capacitors are a sample replica of the input waveform during that period (albeit slightly distorted due to the non-linear charging of the capacitors).

If successive cycles of the input waveform and the switching cycle occur in the same phase relationship, then the voltage on each capacitor will eventually become equal to the input voltage at a particular point along the waveform. No further charging of the capacitors will occur, and the input signal will be available at the output. This is true for the frequency at which one cycle of the input frequency is equal to the switching cycle time, and also for multiples of that frequency.

At other frequencies the signal is heavily attenuated. Consider what happens when a half-cycle of the input waveform is equal to the switch cycle time. Imagine that on the positive half-cycle the peak of the input waveform is stored on C4 in figure 2. During the negative half-cycle S4 will be closed at the trough of the waveform. The net voltage on C4 will be zero. This is true for the other capacitors, so the output signal is zero. This will also occur at all frequencies

1



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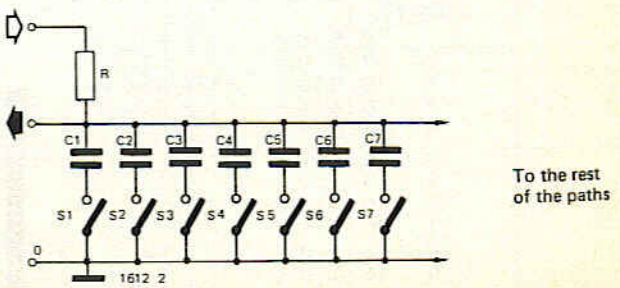


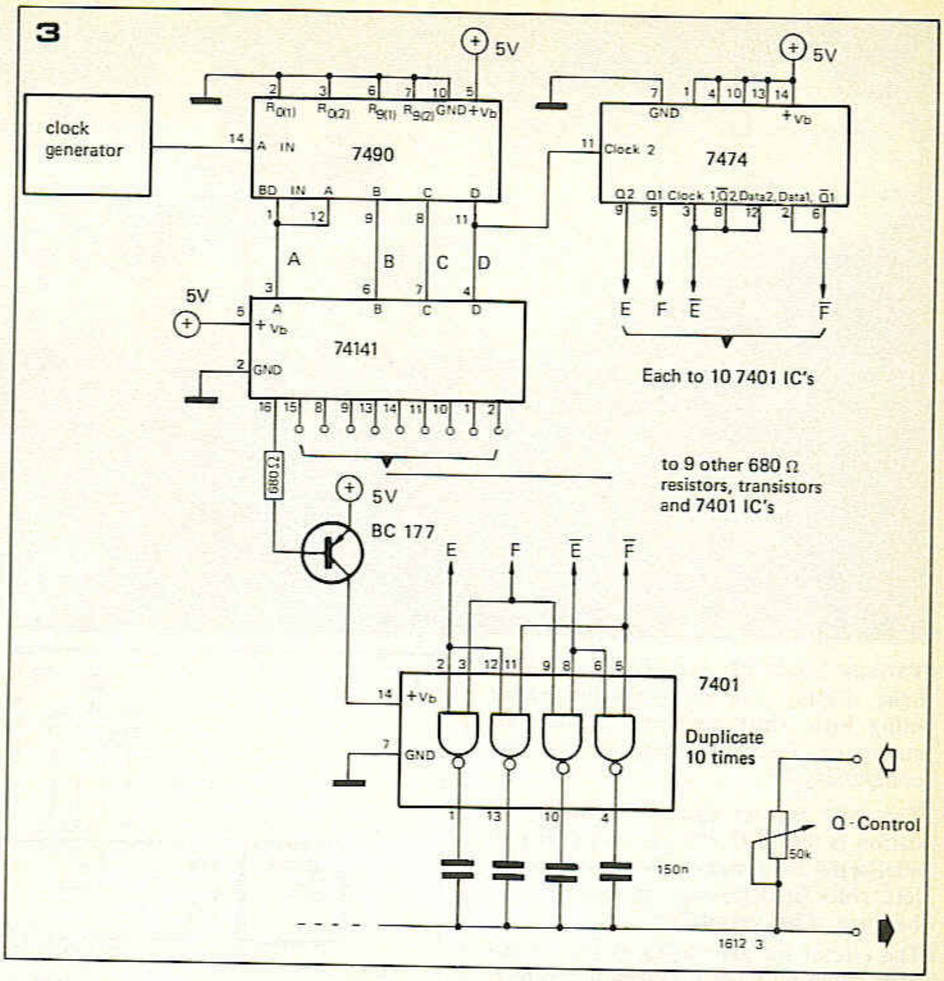
where an odd number of half-cycles is equal to the switch cycle time.

In practice, of course, the switching is accomplished electronically, for example by a ring counter. The result is a comb filter whose rejection frequencies can be varied by varying the clock frequency of the ring counter. The Q-factor can be altered by the single input resistor, R. Distortion of the output signal may be reduced by increasing the number of 'paths', i.e. the number of capacitors.

A practical realisation of a 40-path filter is shown in figure 3. A 7490 decade counter and a 7474 dual D-flip-flop form a divide-by-40 counter. The outputs of the 7474 are decoded by ten 7401 packages, each of which switches four capacitors, making 40 in all. The outputs of the 7490 are decoded by a 74141 BCD-to-decimal decoder/driver and used to switch the supplies to the 7401's via PNP transistors. The capacitors are thus arranged in a 4 x 10 matrix, and are switched as follows:

At the start of a cycle the outputs of the 7474 are all '0' so the capacitors connected to pin 4 of each 7401 are switched in sequence as the 7490 counts from 0 to 9 and the supplies to each 7401 package are switched in turn. When the count reaches 10 output E of the 7474 becomes '1'.

The capacitors connected to pin 13 of the 7401's are switched as the 7490 counts the second decade, and so on. The Q-control is provided by the 50 k potentiometer. The signal source must have a low output impedance and the output of the filter must be connected to a high impedance load.



Applications

This filter has a very narrow bandwidth, with the Q-control at maximum typically less than a semitone. Various effects can be obtained with the circuit. If a narrow pulse waveform is fed in, chimes or percussion effects can be produced at the output, depending on the control frequency. Aircraft noises and other engine noises can also be simulated by filtering out harmonics of complex tones.

The phasing effect occurs when a clock frequency is used which is higher than the upper limit of the audio spectrum (say 20 to 100 kHz). The Q-control must be set in a fairly high position.

The path filter may also be used with an electronic organ or synthesizer, to produce strange effects. A particularly unusual sound can be obtained by feeding the clock input of the filter from the signal outputs of an electronic organ (squarewave outputs from dividers, before filtering) and by feeding a noise signal into the signal input. The results are, to say the least, unlike any organ in existence.

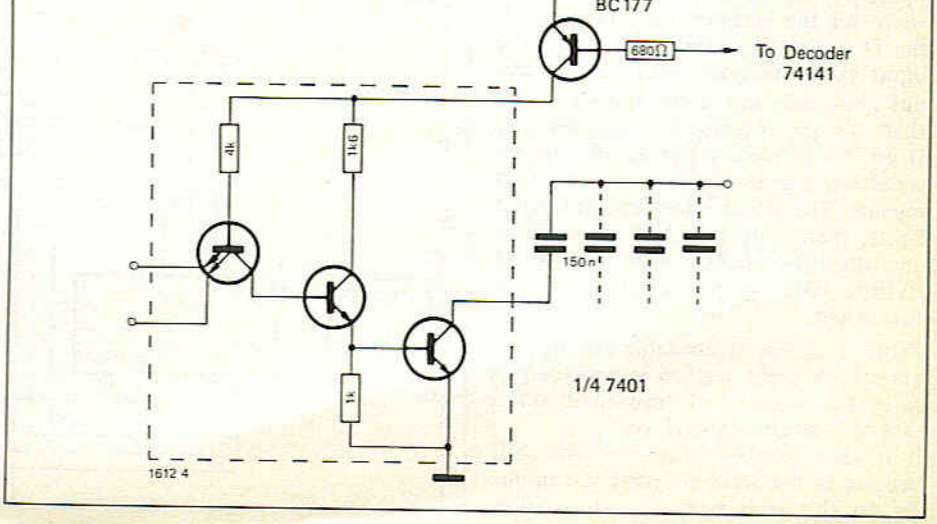
The circuit as described does have its limitations. It will not operate effectively below the frequency whose half-cycle is the same length as the counter cycle. Lowering the clock frequency to compensate for this introduces problems with noise due to the clock frequency and the switching of the supplies to the 7401's. This is aggravated by differences in the characteristics of the 7401's and of the transistors. Increasing the number of stages so that a higher clock frequency may be used will overcome many of these problems. ◼

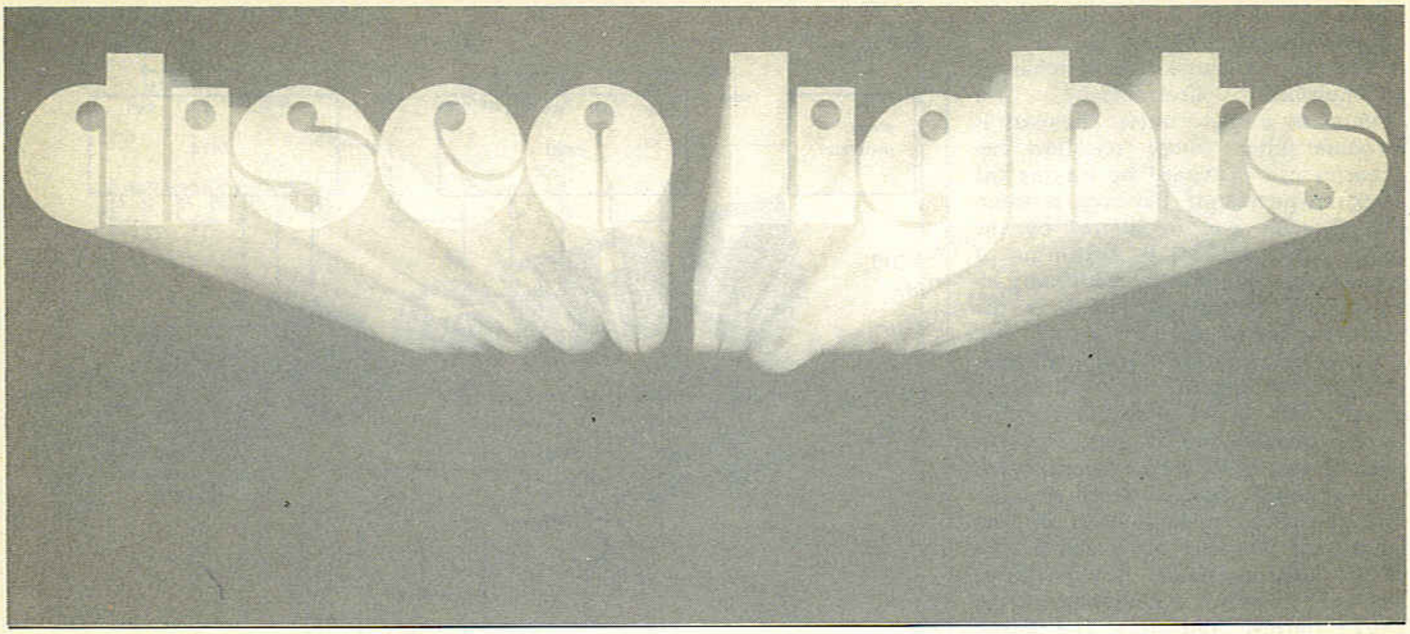
Figure 1. Frequency response of a comb filter. Frequencies phase-shifted by odd multiples of 180° are almost completely rejected.

Figure 2. Principle of a path filter. All capacitors have the same value and the number of capacitors may be optionally increased almost indefinitely.

Figure 3. Circuit for a practical path filter. The 7401 and the associated supply switching transistor are duplicated 10 times. Each 7401 is connected to the outputs of the 7474 as shown.

Figure 4. Showing the internal circuitry of one gate in a 7401 package, and how each capacitor is connected.





Various kinds of psychedelic flashing light display can be generated easily using logic shift registers. Several circuits are discussed here of varying complexity.

The shift register chosen for this application is the 7495. This is a four-bit parallel/serial load, parallel/serial out, shift-left, shift right register, and was chosen because of its versatility.

The circuit for generating a type of display commonly used is given in figure 1. Four lamps light in sequence until all are lit, then all are extinguished simultaneously. The circuit operates as follows: The outputs A to D of the shift register are initially at '0' so the mode control input (pin 6) is low. In this mode serial data is entered at pin 1 and is shifted one place right on each clock pulse. Since the serial input is held high by the 1 k resistor, outputs A to D successively go high until all are high. When output D goes high the mode control goes high with it and the shift register is now in the parallel load, shift left mode. The parallel inputs A to D are grounded so that '0's are entered and subsequently appear on the outputs. The cycle then repeats. A truth table for the sequence is given in Table 1.

Figure 2 is a variation on the circuit of figure 1. Instead of changing the mode when all the outputs have become '1' the D output is connected to the serial input via an inverter. When the D output goes high this input is held low so that '0's are entered. The outputs A to D go low in turn. When all are low the serial input goes high and the sequence repeats. The visual effect is that lamp A lights, then lamp B and so on until all are lit. The lamps then extinguish starting with lamp A until all are extinguished.

Table 2 is the truth table for this sequence. A reset button is provided to clear the register of unwanted states that may occur at switch-on.

It is also possible to operate the shift register in the serial in, shift left mode. To do this it is necessary to connect

1

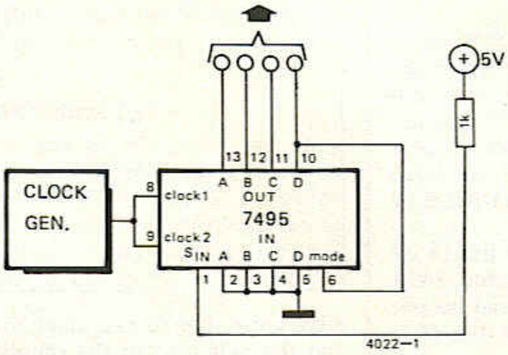


Table 1

clock	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	0	0	0

2

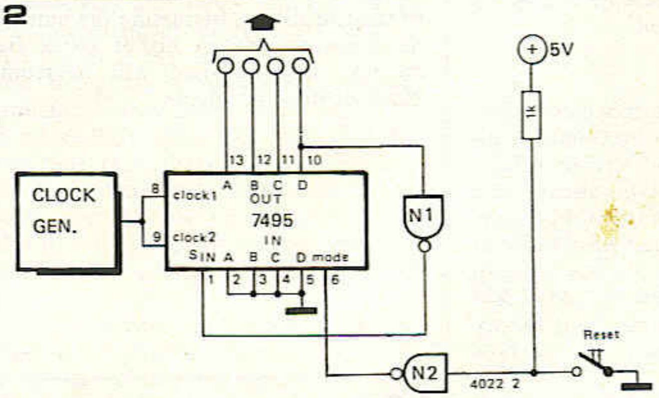


Table 2

clock	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

3

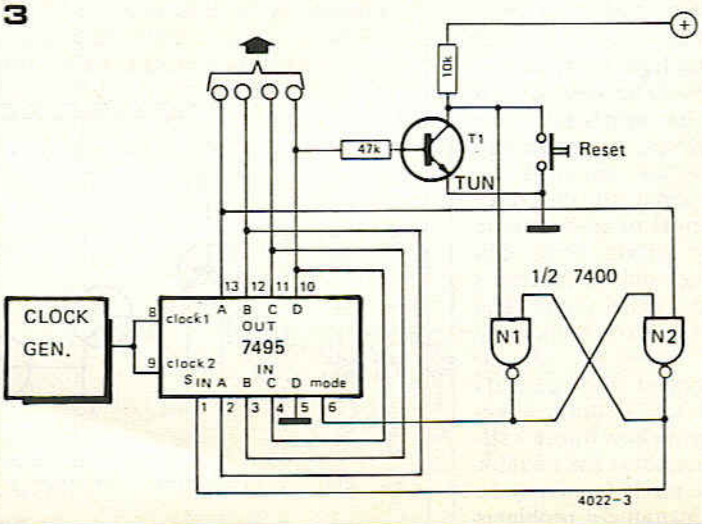


Table 3

clock	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	1	1	1	0
6	1	1	0	0
7	1	0	0	0
8	0	0	0	0

Figures 1-5. These five basic circuits show the versatility of the 7495. Each circuit gives a different output sequence.

Tables 1-5. These tables show the output sequences of the corresponding circuits

Figure 6. One way of isolating the control circuitry from the triac is to use transformers. The input to this circuit is TTL compatible.

4

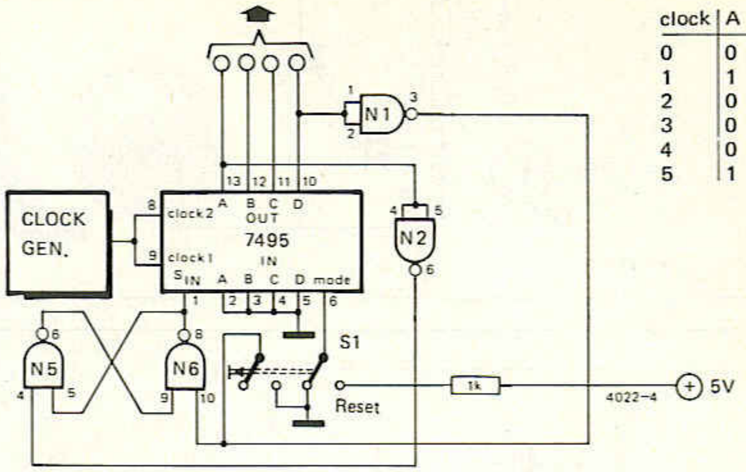


Table 4

clock	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0

5

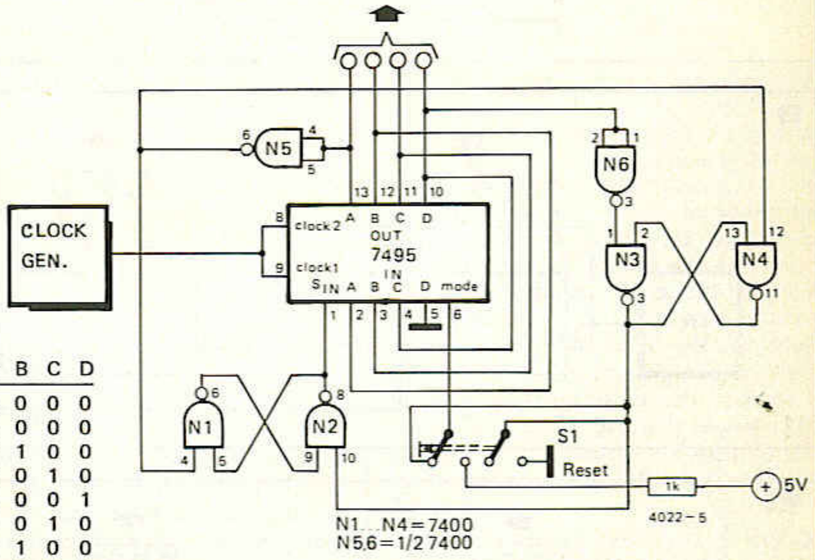
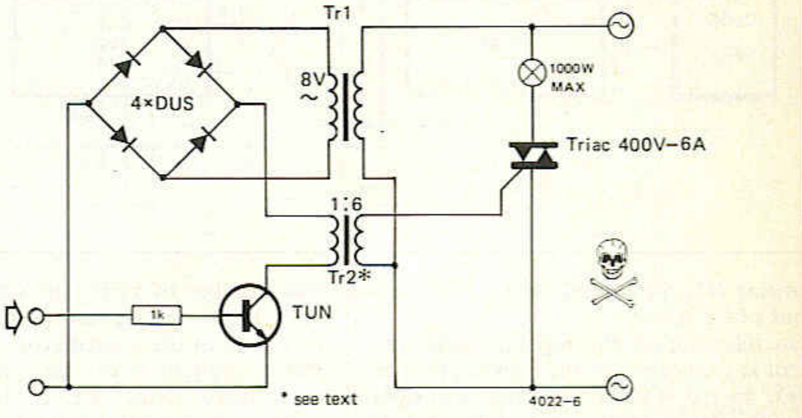


Table 5

clock	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	1	0
6	0	1	0	0
7	1	0	0	0
8	0	1	0	0

6



each output to the preceding input (D to C, C to B, B to A). Serial data is then entered at the D input and is shifted left on each clock pulse.

This may be used to make a display where the lamps light in the order A to D, then extinguish in the order D to A, as in figure 3. This circuit operates as follows: the flip-flop N1, N2 is initially set so that the serial input is high and the mode control is low.

'1's are thus entered at the serial input and appear successively at the outputs A to D. When output D becomes high T1 is turned on and the flip-flop is reset. The mode control input becomes '1', reversing the shift direction. Since the D input is grounded the data entered is '0', so the outputs go low starting with the D output. When all the outputs are low the flip-flop is set and the sequence repeats. The truth table is given in table 3.

The circuits so far discussed are similar in that after four clock pulses all lamps are lit. It is, however a simple matter to devise a circuit where the lamps light in sequence but only one at a time, by circulating a single '1' through the shift register.

In the circuit of figure 4 the lamps light in the sequence A to D, with only one lamp at a time being lit. When lamp D extinguishes lamp A lights and the sequence repeats (table 4). The circuit operates as follows: on switching on the A to D outputs will set randomly so that more than one output may be high. This would mean that a number of '1's would be circulating, whereas only a single '1' is required. For this reason a reset button is provided. When S1 is depressed the flip-flop comprising N5 and N6 is set, taking the serial input high. At the same time the mode control is taken high by the other half of S1, so that on the next clock pulse the register shifts the '0's from the grounded A to D inputs to the corresponding outputs, clearing the register.

When the switch is released the register is in the serial-in, shift right mode, so on the next clock pulse the '1' present on the serial input will appear at output A. The output of N2 will go low, resetting the flip-flop N5, N6 so that the serial input is low. On each successive clock pulse the '1' on the A output is shifted one place to the right until it appears at output D. When this occurs the output of N1 goes low, setting the flip-flop. A '1' now appears at the serial input, and the process repeats.

Figure 5 shows a variation on this circuit, in which a '1' travels back and forth from one end of the register to the other (table 5). The circuit is initially reset by pressing S1. This sets the flip-flop N1, N2 so that a '1' appears at the serial input. It also puts the register in the shift-left mode, so that the '0' on the grounded D input is shifted left, clearing the register. The flip-flop com-

7

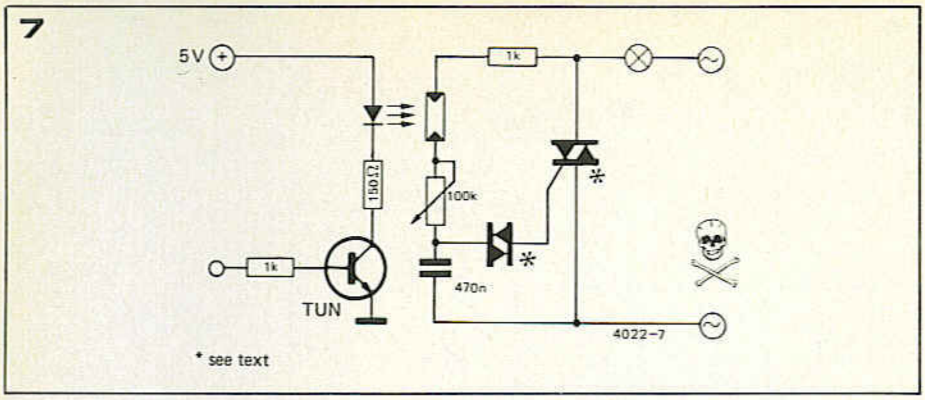


Figure 7. A more elegant solution is to use opto-isolation.

8

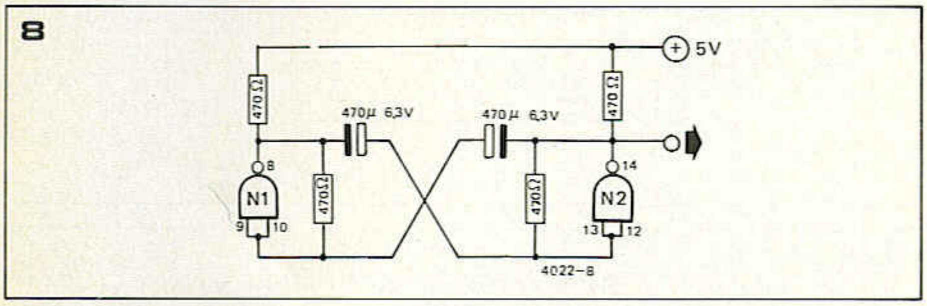


Figure 8. Two NAND gates (or inverters) can be connected as an astable multivibrator. This provides a simple clock generator circuit to drive the 7495.

9

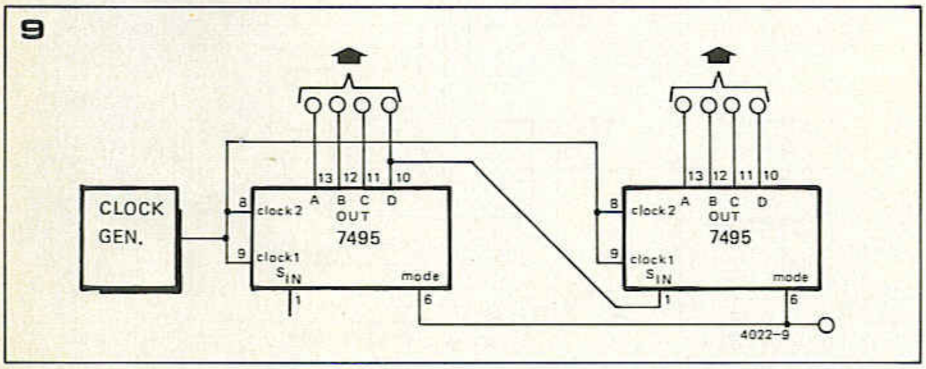


Figure 9. If four outputs are considered insufficient, circuits 1, 2 and 4 can be extended ad infinitum in this way.

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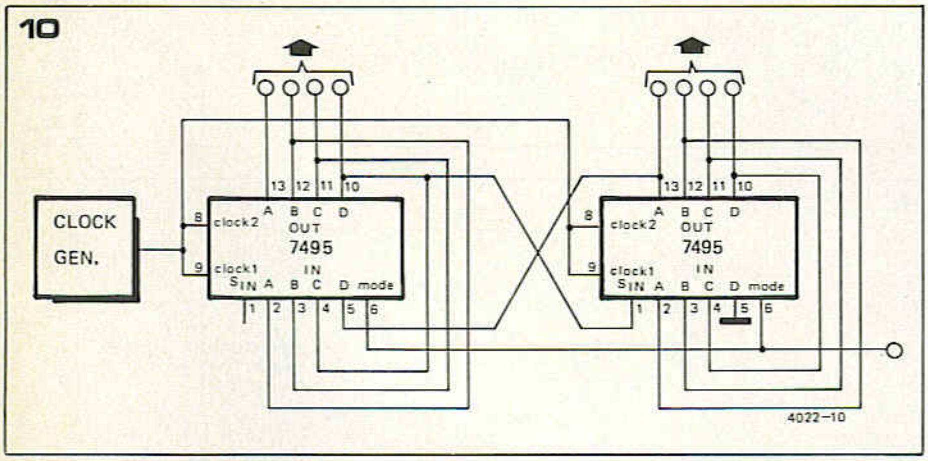


Figure 10. Circuits 3 and 5 can also be readily extended to give any number of additional outputs.

prising N3, N4 is reset, so that the output of N3 is low.

On releasing S1 the register mode control is connected to the (low) output of N3, so the register is in the shift-right mode. On the first clock pulse the '1' applied to the serial input appears at the A output. It is inverted and resets the flip-flop N1, N2 so that no more '1's are entered. The '1' which is in the register is shifted right on each successive clock pulse until it reaches the D output. Flip-flop N3, N4 is then set, reversing the shift direction. When the '1' again reaches the A output flip-flop N3, N4 is reset and the shift direction again reverses, and so on.

The number of variations on these circuits is, of course, limited only by the ingenuity of the constructor.

Actual switching of the lamps is accomplished using triacs. Unless the entire circuitry is housed in an insulated box the logic circuitry must be isolated from the mains. This may be accomplished by either transformer or optical isolation of the control circuitry from the triac, and suitable circuits are given in figures 6 and 7.

In figure 6 the secondary voltage of Tr1 is full-wave rectified and applied to the collector of the transistor via the primary of Tr2. When the transistor is turned on by one of the outputs of the register, current flows through the primary of Tr2 and the current induced in the secondary triggers the triac. The choice of transformers is not critical. Tr1 can be a small bell transformer, whilst Tr2 should have a ratio of about 1 : 6 and can be a miniature type since only a small current flows through it. Of course Tr1 and the bridge rectifier are required only once in the circuit, but the transistor, Tr2 and the triac must be repeated for every output from the shift register. With this circuit triggering of the triac is not optimum. Phasing of the transformers is important, so if the circuit does not work first time reverse the polarity of one of the windings.

A more elegant solution is to use opto-isolation, as in the circuit of figure 7. This is simply a conventional triac dimmer with the main potentiometer replaced by a light-dependent resistor housed in a light-tight enclosure with a LED. When the transistor is turned on by an output of the shift register the LED lights and the illumination causes the resistance of the LDR to fall. The triggering point of the triac is thus advanced and the lamp lights.

The base current of the transistor in both these circuits is about 3 mA, so they can easily be driven by the outputs of the shift register. The choice of diac and triac for both these switches depends on the maximum load to be switched.

A simple clock generator circuit is given in figure 8. This is simply two NAND-gates or inverters connected as an astable multivibrator. A variable frequency pulse generator could also be used so that the travelling speed of the light pattern could be altered. Figures 9 and 10 show how the discolights may be extended with several shift registers. Figure 9 is intended for extension of figures 1, 2, and 4, and figure 10 for the extension of figures 3 and 5.

ota

The OTA (Operational Transconductance Amplifier) is a new type of operational amplifier which was introduced by RCA a few years ago. The most important difference from a normal operational amplifier is that an OTA does not work as a voltage amplifier but as a voltage-driven current source. The gain can be determined externally by the value of the output load resistor, and by the so-called bias current. The latter makes it possible to control the gain instantaneously over a range of about 80 dB by an external potential. Since the OTA will be used in several Elektor projects, an explanation of the working principles of this device should prove useful.

As the gain in an OTA can be controlled by the current from an external source (the bias current I_{ABC}), possibilities are opened up for new applications which have up to now been difficult to perform satisfactorily with discrete components. A simple application of the OTA, for example, is amplitude modulation. Although it is basically possible to effect this with one or more discrete transistors, closer inspection shows that discrete circuits do not achieve all forms of amplitude modulation really satisfactorily. Tremolo (amplitude modulation of a signal which is to be reproduced acoustically) is not easy to achieve electronically without relatively high distortion or interference. Other applications of the OTA such as multiplexing or sampling of signals are more successful than with other methods because of the OTA's high slew rate of 50 V/μsec. Automatic volume control is also an obviously attractive application for OTAs. More applications of two types of OTA, the CA 3080 and the CA 3094 AT, will be given in future issues. These are the most interesting of the large range of OTAs which have been developed by RCA. The CA 3094 AT has in fact been developed from the CA 3080, and the only basic difference concerns the output circuit.

Linear transconductance (forward slope)

Before using the OTA in practical circuits, it is important to understand the meaning of the term 'forward slope' for which the abbreviation 'g_m' is used. The term g_m is expressed in mho (1/Ω) or millimho ($\frac{1}{\Omega x 10^3}$). The amplification factor of a normal operational amplifier (known as a voltage amplifier) corresponds to the g_m of a voltage-driven current source (i.e. an OTA). The relationship between the output current and the corresponding input voltage of an OTA is:

$$\Delta I_{out} = g_m \times \Delta V_{in}.$$

The output signal of an OTA is thus a current which is proportional to its g_m. The output voltage (ΔV_{out}) appearing as a result of the output current, ΔI_{out}, in an OTA is the product of this current and the load resistor.

CA 3080

Figure 1 shows a simplified circuit of the CA 3080. T_1 and T_2 in figure 1 form a differential amplifier, which is also found in most normal operational amplifiers. W, X, Y and Z are known as current mirrors. A current mirror consists in principle of two transistors, one of which is connected as a diode. Figure 2 gives the circuit of a current mirror of this type. As the transistors T_a and T_b are supposedly identical, a current I' into T_a results in a second current I into T_b with the following relationship to I':

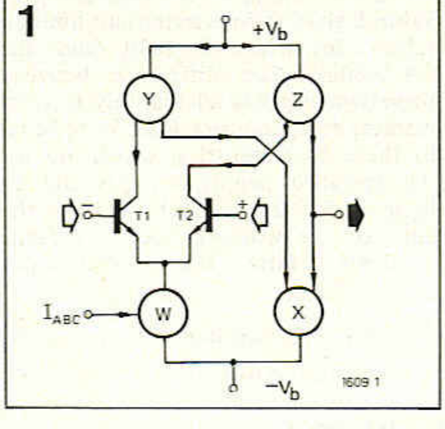
$$\frac{I}{I'} = \frac{\alpha'}{\alpha' + 2}$$

In this formula α' is the current amplification of transistors T_a and T_b. A current mirror can be regarded in practice as a current source in which the output current (I) is almost identical to the control current (I'), and in which the two currents I and I' can in fact be regarded as isolated from one another.

A disadvantage of the current mirror as shown in figure 2 is that it is sensitive to small differences in the current amplifications of transistors T_a and T_b, these differences resulting in the currents I' and I not being precisely equal. This effect can be greatly reduced by the inclusion of a third transistor (T_1 in figure 3).

Current mirror W in figure 1 has the circuit shown in figure 2, while current

1



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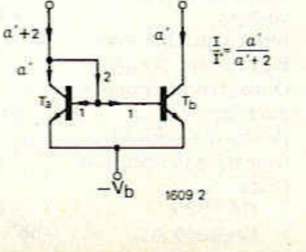

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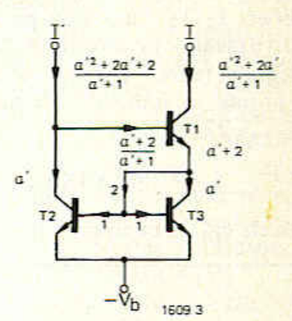
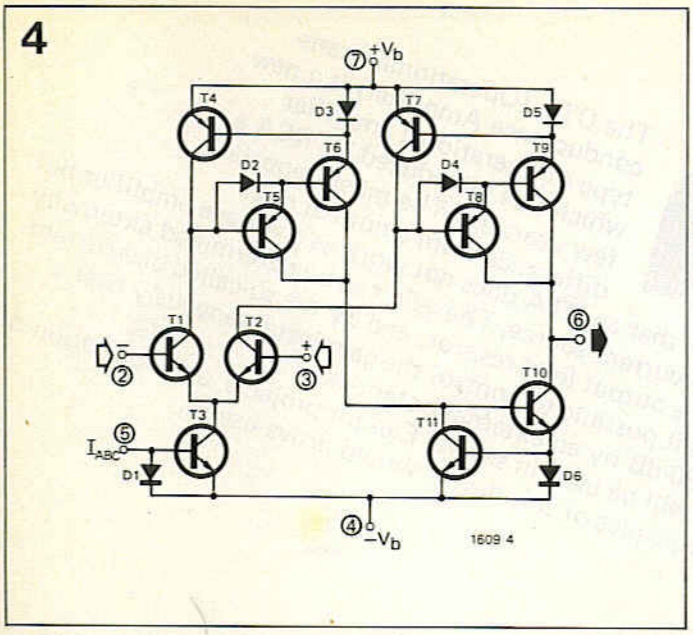


Figure 1. Simplified circuit of the CA 3080. Transistors T_1 and T_2 form the differential input amplifier. W, X, Y and Z are so-called current mirrors.

Figure 2. A current mirror can be simply made up with two transistors (T_a and T_b). The drive current I' gives rise to a current I which is proportional to I'.

Figure 3. The current mirror of figure 2 is sensitive to differences between the current gains of the two transistors (T_a and T_b). Addition of T_1 reduces this sensitivity considerably.

4



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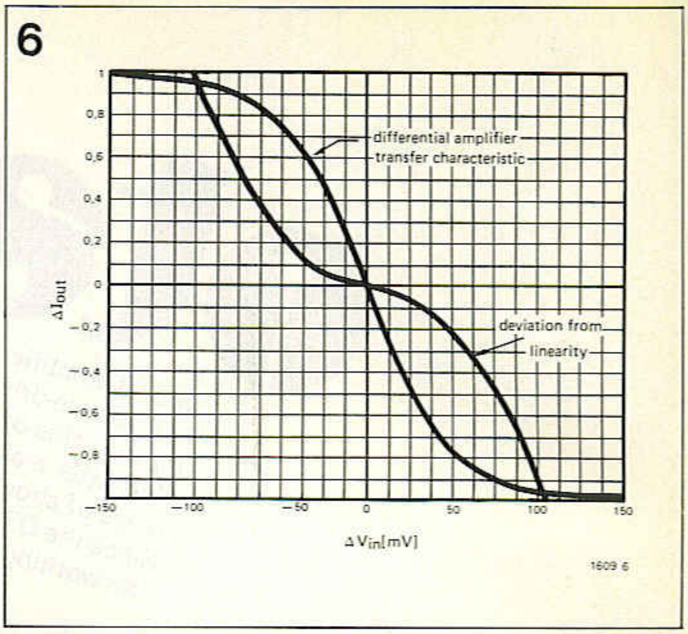

mirrors X, Y and Z are as shown in figure 3. It should also be noted that Y and Z have PNP transistors.

The complete circuit diagram of the CA 3080 is given in figure 4. The circled points indicate the connection numbers in the TO-5 housing. This housing, as seen from the upper side, is shown diagrammatically in figure 5.

In one of the RCA data sheets a drawing corresponding to figure 5 shows the reference tip between connections 1 and 8. This can lead to confusion: the drawing in figure 5 is correct.

In the circuit shown in figure 4, T_1 and T_2 are the differential input amplifier. Transistor T_3 is the common emitter impedance of this differential amplifier. The most significant difference from the input stage of a normal opamp is that T_3 is part of a current mirror, so that its collector current is equal to the bias current (I_{ABC}). The value of the collector current of T_3 determines the emitter current of the differential amplifier T_1/T_2, and this provides an effective means of controlling the overall transconductance. The g_m of an OTA in normal ambient temperatures (16°C . . . 27°C) is given by:

$$g_m = 19.2 \times I_{ABC}$$

in which g_m is expressed in millimhos ($1/\Omega \times 10^{-3}$) and I_{ABC} in mA.

In figure 4 the output signal of the OTA is taken from the collectors of T_9 and T_{10} (connection 6) which form part of the current mirrors Z and X respectively in figure 1. As I_{ABC} is varied, the g_m of the OTA changes and therefore the output current does likewise; hence:

$$\Delta I_{out} = g_m \times \Delta V_{in} = 19.2 \times I_{ABC} \times V_{in}$$

(at normal temperatures!)

The OTA can easily be made to operate as a voltage amplifier by connecting a load resistor R_L between the output and circuit earth. The output voltage then becomes:

$$\Delta V_{out} = R_L \times 19.2 \times I_{ABC} \times \Delta V_{in}$$

in which I_{ABC} is in mA, R_L is in kΩ, V_{out} and V_{in} are in volts.

Characteristics of the CA 3080

Table 1 gives various important limiting values for the CA 3080 and the CA 3080 A. The difference between these two types is related only to their working temperature ranges. In addition to these characteristics, which are for the specified supply voltages and an I_{ABC} of 500 µA, it can be said that the limit of the working frequency range is about 2 MHz. The quoted input

Figure 4. Complete circuit of the CA 3080 IC. The circled numbers correspond to the coding of the connecting leads.

Figure 5. Connections for the CA 3080 IC are the same as on the µA 709 except for Pins 1 and 5.
The drawing shows the top view of the IC.

Figure 6. These curves show changes in output current (ΔI_{out}) plotted as functions of changes in the input voltage (ΔV_{in}).

Figure 7. Input resistance (R_{in}) as a function of the so-called bias current (I_{ABC}).

Figure 8. As with the input resistance, the output resistance of the CA 3080 is dependent on the bias current I_{ABC}. As figure 7 and this graph show, both relationships are completely linear.

Figure 9. The CA 3080 connected as a D.C.-coupled differential amplifier. Gain can be varied by potmeter P_1 from about 30 to about 100 times.

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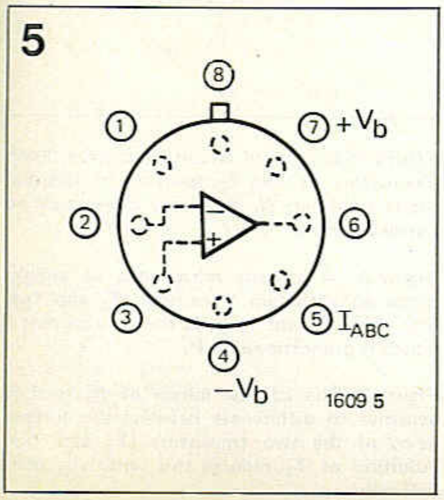

Table 1. Characteristics and maximum rating of the CA 3080 and CA 3080 A ICs.

Maximum ratings:	
DC supply voltage between $+V_b$ and $-V_b$:	36 V
Differential input voltage:	± 5 V
Common mode input voltage:	$+V_b$ to $-V_b$
Input signal current:	1 mA
Bias current (I_{ABC}):	2 mA
Output short-circuit duration:	no limitation
Device dissipation:	125 mW
Operating temperature range:	
CA 3080	0° to 70°C
CA 3080 A	−55° to +125°C

Characteristics: (V_b = +15 V; $-V_b$ = −15 V; I_{ABC} = 500 µA)	
Input capacitance:	3.6 pF
Input resistance:	26 kΩ
Input offset current:	0.2 µA
Input bias current:	2 µA
Slew rate with unity gain:	50 V/µS
Transconductance (g_m):	9600 µmho
Output resistance:	15 MΩ
Peak output current:	500 µA
Peak output voltage:	
positive	13.5 V
negative	−14.4 V
Amplifier supply current:	1 mA
Device dissipation:	30 mW

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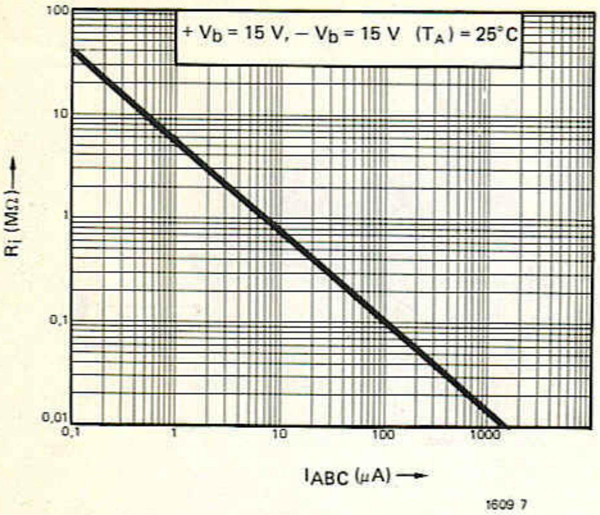

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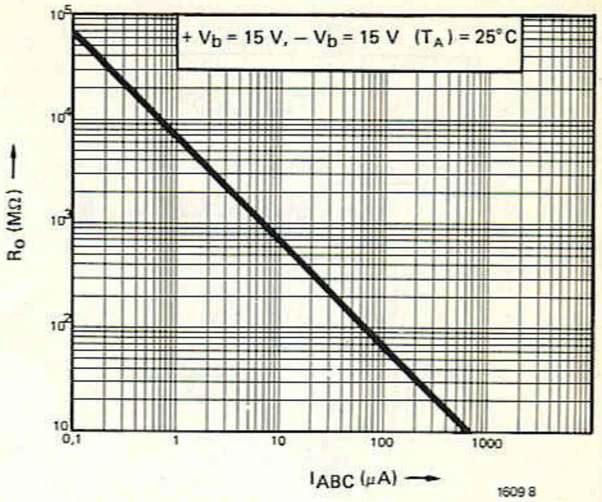


resistance of 26 k is dependent on the value of I_{ABC}.

If a value of 1 MΩ is chosen for the output load resistor, the voltage gain is easy to work out from the characteristics given in table 1:

$$A = \frac{\Delta V_{out}}{\Delta V_{in}} = R_L \times g_m$$

$$= 10^6 \times 9.6 \times 10^{-3} \approx 80 \text{ dB}$$

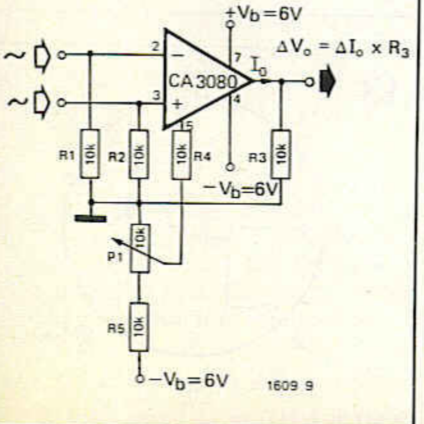
It can be deduced from this last formula that the voltage gain can also be varied by changing the load resistance.

The curves in figure 6 show that the overall characteristic of the CA 3080 is completely linear for small inputs to the differential amplifier. The curves show the relative values of ΔI_{out} and the deviations from linearity as functions of the relative values of ΔV_{in}. Figure 7 shows the input impedance of the CA 3080 as a function of the bias current I_{ABC}. The maximum impedance attainable in this OTA is about 40 MΩ with a bias current of 0.1 μA.

The output impedance is also, of course, dependent on the value of I_{ABC}. Figure 8 shows that this relationship is linear.

For the sake of completeness, it should be said that the characteristic of figure 7 also holds good for the CA 3094 AT. Figure 8 also holds good for the CA 3094 AT, but only for its current output. This IC has other outputs.

9



OTA - opamp

Figure 9 shows a practical circuit for the CA 3080 from which a comparison can be made with normal opamps.

The power supply is symmetrical at ± 6 V. Both inputs are D.C.-coupled and are connected to chassis earth through R_1 and R_2 respectively. Resistor R_3 of figure 9 is introduced in order to obtain voltage amplification, as in an opamp. The usual feedback from the output to the inverting input of the IC is missing, because the gain can be controlled by the bias current I_{ABC} at pin 5. I_{ABC} is easy to calculate. While recalling that the emitter of T_3 is connected to $-V_b$ (pin 4), assume that I_{ABC} is drawn via a resistor R_x from chassis earth, which is 6 V positive in relation to $-V_b$. The relationship then becomes:

$$I_{ABC} \approx \frac{V_b - 0{,}7}{R_x}.$$

In this formula, I_{ABC} is in mA, while V_b is in volts and R_x is in kΩ. The quantity 0.7 is the base-emitter potential of T_3 in figure 4. To find the value of R_x for a desired value of I_{ABC}, the formula can, of course, be rewritten:

$$R_x \approx \frac{V_b - 0.7}{I_{ABC}}.$$

In figure 9 R_x is replaced by the combination R_4, R_5 and P_1. When the slider of P_1 is at the positive end of its travel (i.e. at 0 V), the voltage across the series connection of R_x and the base-emitter junction of T_3 is V_b, so that

$$I_{ABC} = \frac{V_b - 0.7}{R_4} \approx 0.53 \text{ mA}.$$

It therefore follows that the voltage gain is:

$$A = R_3 x g_m x I_{ABC} \approx 10 x 19.2 x 0.53 \approx 100.$$

When, however, the slider of P_1 is at the negative end of its travel (the junction of R_5 and P_1), the voltage relative to $-V_b$ at the slider of P_1 is:

$$V_x \approx \frac{R_4 /\!/ P_1 \times (V_b + 0.7\,\frac{R_5}{R_4})}{R_4 /\!/ P_1 + R_5}$$

$$= \frac{5 \times 6.7}{15} \approx 2.2 \text{ V}$$

The effective voltage across R_4 is therefore:

$$2.2 \text{ V} - 0.7 \text{ V} = 1.5 \text{ V}$$

so the bias current is given by:

$$I_{ABC} \approx \frac{1.5}{10} \text{ mA} = 0.15 \text{ mA}.$$

The voltage gain is therefore:

$$A \approx R_3 x g_m x I_{ABC} \approx 10 x 19.2 x 0.15 = 29X$$

If the gain of this IC is allowed to drop substantially, considerable distortion may result unless special attention is given to the design of the differential inputs. Should the input transistors T_1 and T_2 (figure 4) not be exactly matched, their emitter currents will differ when I_{ABC} is low, and this will cause distortion. In this connection, the following rules of thumb apply:

a. If the OTA gain is fixed, resistors R_1 and R_2 (figure 9) must have values which are lower, by a factor of at least 2 : 1, than the value of input impedance read from figure 7 for the relevant value of I_{ABC}.
b. R_1 and R_2 must have the same value when I_{ABC} is less than about 0.5 μA.
c. For fixed gain with values of I_{ABC} between 1 μA and 10 μA, the values of resistors R_1 and R_2 may differ by a factor of 2.
d. When I_{ABC} is over 10 μA, R_1 and R_2 may differ in value by a factor of 4.
e. If the gain is to be variable over a range greater than 1 : 5, resistors R_1 and R_2 must have values lower, by a factor of at least 2, than the

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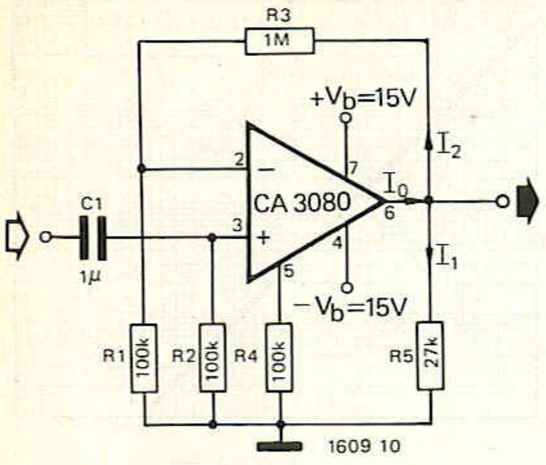

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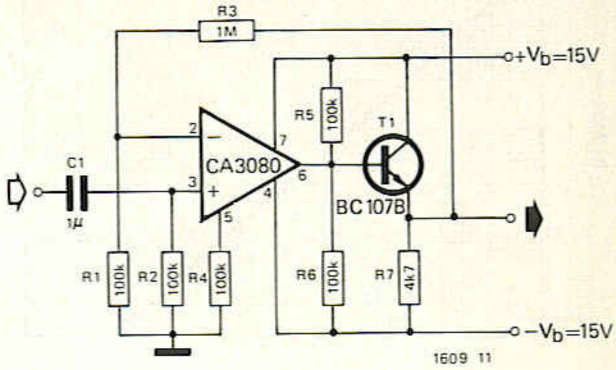

value of input impedance, indicated by figure 7, for the maximum I_{ABC}.

Negative feedback

Negative voltage feedback can be used with an OTA as it can with a normal opamp. Figure 10 gives an example of a circuit for a CA 3080. The bias current I_{ABC} is determined by R_4. The potential across this resistor is the negative power supply (15 V), less the 0.7 V base-emitter voltage which was discussed in relation to T_3 of figure 4. In this case the value of bias current is given by:

$$I_{ABC} = \frac{15 - 0.7}{10^5} = 143\ \mu A$$

so that g_m works out at

$$19.2 \times I_{ABC} = 2.74 \text{ mmho}.$$

The voltage gain given by a CA 3080 in the circuit shown in figure 10 is not determined solely by the value of the load resistor R_5, but also by R_1 and R_3. In the first place, the effective output load resistance is R_5 and $(R_3 + R_1)$ in parallel. In the second place, the voltage developed at pin 6 across this effective output load is fed back to the inverting input (pin 2) with a step-down ratio $R_1/(R_1+R_3)$.

The effective voltage gain between the input and pin 6 is thus:

$$A_f = \frac{A_o}{1 + (A_o \cdot f)} = \frac{g_m \cdot R_L}{1 + (g_m \cdot R_L \cdot f)}$$

$$= \frac{g_m \cdot [(R_1 + R_3) /\!/ R_5]}{1 + g_m\,[(R_1 + R_3) /\!/ R_5] \cdot \dfrac{R_1}{R_1 + R_3}}$$

$$\approx \frac{g_m \cdot R_5}{1 + g_m \cdot R_5 \cdot \dfrac{1}{11}} \approx 10x$$

(f is the feedback factor $\frac{R_1}{R_1 + R_3}$.)

It can be seen from figure 10 that if R_3 is omitted there will be no voltage feedback from the output. This is equivalent to making R_3 infinitely large in the foregoing calculations, and results in in the voltage gain being increased by a factor of about 8.

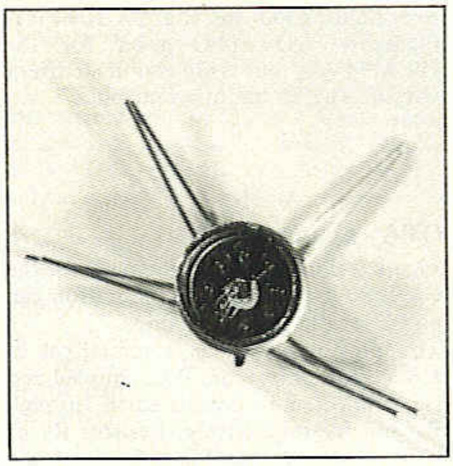

Table 2. Characteristics and maximum ratings of the CA 3094 AT.

Maximum ratings:	
DC supply voltage between $+V_b$ and $-V_b$:	36 V
Differential input voltage:	±5 V
Common mode input voltage:	$+V_b$ to $-V_b$
Input signal current:	1 mA
Bias current (I_{ABC})	2 mA
Output current:	
peak:	300 mA
average:	100 mA
Device dissipation:	
without heat sink:	630 mW
with heat sink:	1.6 W
Peak dissipation (1 mS):	10 W
Operating temperature range:	−55° to +125°C
Characteristics:	
($+V_b$ = 15 V; $-V_b$ = −15 V; I_{ABC} = 100 µA).	
Differential input capacitance:	2.6 pF
Differential input resistance: (I_{ABC} = 20 µA):	1 MΩ
Input offset current:	0.02 µA
Input bias current:	0.2 µA
Device dissipation:	10 mW
Bandwidth (Unity gain):	30 MHz
Amplifier bias voltage:	0.68 V

If a comparison is now made between the circuit of figure 10 and a normal opamp, such as the µA 741, a number of similarities become evident. Both the OTA and the opamp can be operated as voltage amplifiers, and voltage negative feedback can be used with either. Both can have either symmetrical or asymmetrical inputs, inverting or non-inverting. The OTA, however, becomes a pure current source when it has no load resistance; a feature which can be advantageous for some applications. Besides this, the OTA has the feature that, as the transconductance is varied by varying the bias current, the input and output impedances also vary over

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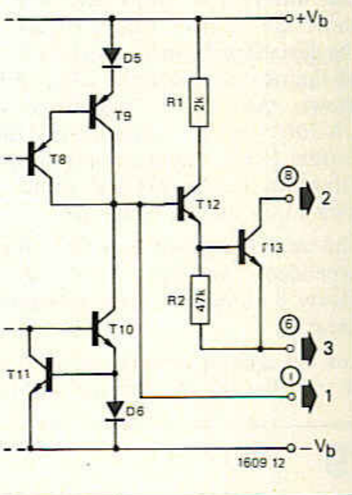

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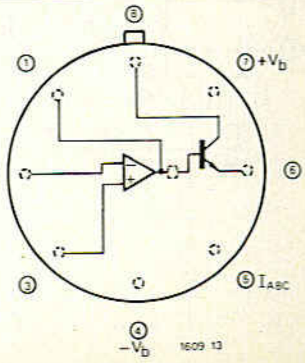


Figure 10. This circuit incorporates negative feedback from the output through R_3 to the inverting input.

Figure 11. A CA 3080 connected as an A.C.-coupled asymmetrical amplifier. Negative feedback is taken from the emitter of T_1 through R_3 to the inverting input of the IC.

Figure 12. Detailed circuit of the output section of a CA 3994 AT OTA. The difference from the CA 3080 consists of the addition of resistors R_1/R_2 and transistors T_{12}/T_{13}.

Figure 13. Functional diagram of the CA 3094 AT. The corresponding output of the CA 3080 (Pin 6) is connected in this case to Pin 1.

a wide range. If it is important for a particular application that one of these parameters (but not the other two) should have a specific value, it can be adjusted to this value by controlling the bias current.

Yet another feature possessed only by the OTA is that the gain can be controlled as may be required by D.C. or A.C. potentials, thus making amplitude modulation, sampling or switching functions possible.

Output buffer stage

Table 1 shows that the peak output current of the CA 3080 is only 500 μA, and this can be a drawback in a number of applications; moreover a 'power' OTA such as the CA 3094 AT costs twice as much.

A simple solution is given in figure 11, which shows a buffer transistor following the OTA. By this means the output current (ΔI_{out}) of the OTA is multiplied in the same ratio as the current amplification of T_1. Another advantage accruing to the addition of T_1 is that, being an emitter follower, its output impedance is low.

The load impedance which the OTA 'sees' at its output is equal to the values of R_5, R_6 and the input impedance of T_1, all in parallel.

The fact that the CA 3094 AT has been developed shows that RCA themselves have, indeed, given thought to the need for higher output currents. This OTA is equivalent to the CA 3080 except for the addition of two resistors and two transistors. Figure 12 shows in detail the output circuit of a CA 3094 AT. A comparison with figure 4 shows that R_1/R_2 and T_1/T_2 have been added in figure 12. Some of the characteristics of the CA 3094 AT are given in table 2, and the connections are given in figure 13. Pins 8 and 6 become power output points for 'sink' or 'drive' currents respectively. The low-power output, which is at Pin 6 in the CA 3080, is brought out at Pin 1 in the CA 3094 AT.

F. Sax

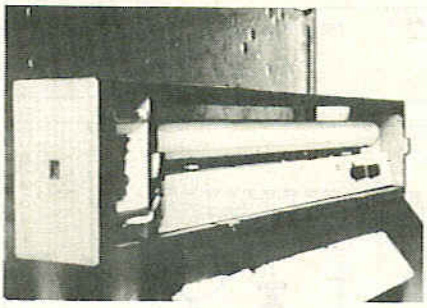
fish feeder

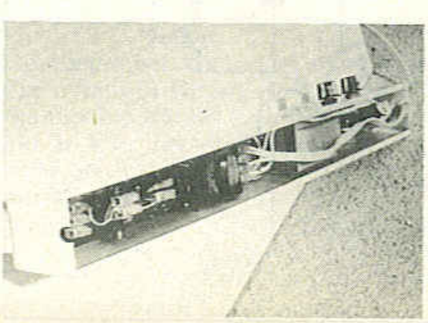
The care of aquaria during holidays can be something of a problem. However the device described here will overcome this problem by automatically dispensing the required quantity of feed each day. The system consists of a light-operated circuit which controls the actual feed dispenser. This senses the change from darkness to light at daybreak each morning, and activates the feed dispenser.

The store of dried feed is held in a trough with V-shaped sides (figure 1). At the bottom of the trough is a cylindrical container which runs the length of the trough, and which has one side cut away. This cylinder is driven, via a reduction gear, from a small model motor. As the container rotates it will fill when the open side is uppermost, and empty into the aquarium as it rotates. The number of revolutions made at each feeding session, and hence the amount of food delivered, is controlled by the electronic circuitry. A cowl at the bottom of the dispenser prevents splashing caused by the fish or the aerator from making the feed sticky and thus clogging the dispenser.

The circuit

In figure 2, T1 is an emitter-follower whose base potential is controlled by a light dependent resistor R1 and a potentiometer P1. This is followed by a Schmitt trigger, T2 and T3, which has a large degree of hysteresis. This drives T4 via R9 and zener diode D2. During darkness the resistance of the LDR is high. The emitter potential of T1 is therefore high, T2 is turned on and T3 is turned off. Hence T4 is also turned on. When daybreak comes the resistance of the LDR drops, the emitter potential of T1 drops, and when the switch off threshold of the Schmitt trigger is reached T2 turns off and T3 turns on. T4 therefore turns off. Point A goes up to supply potential.



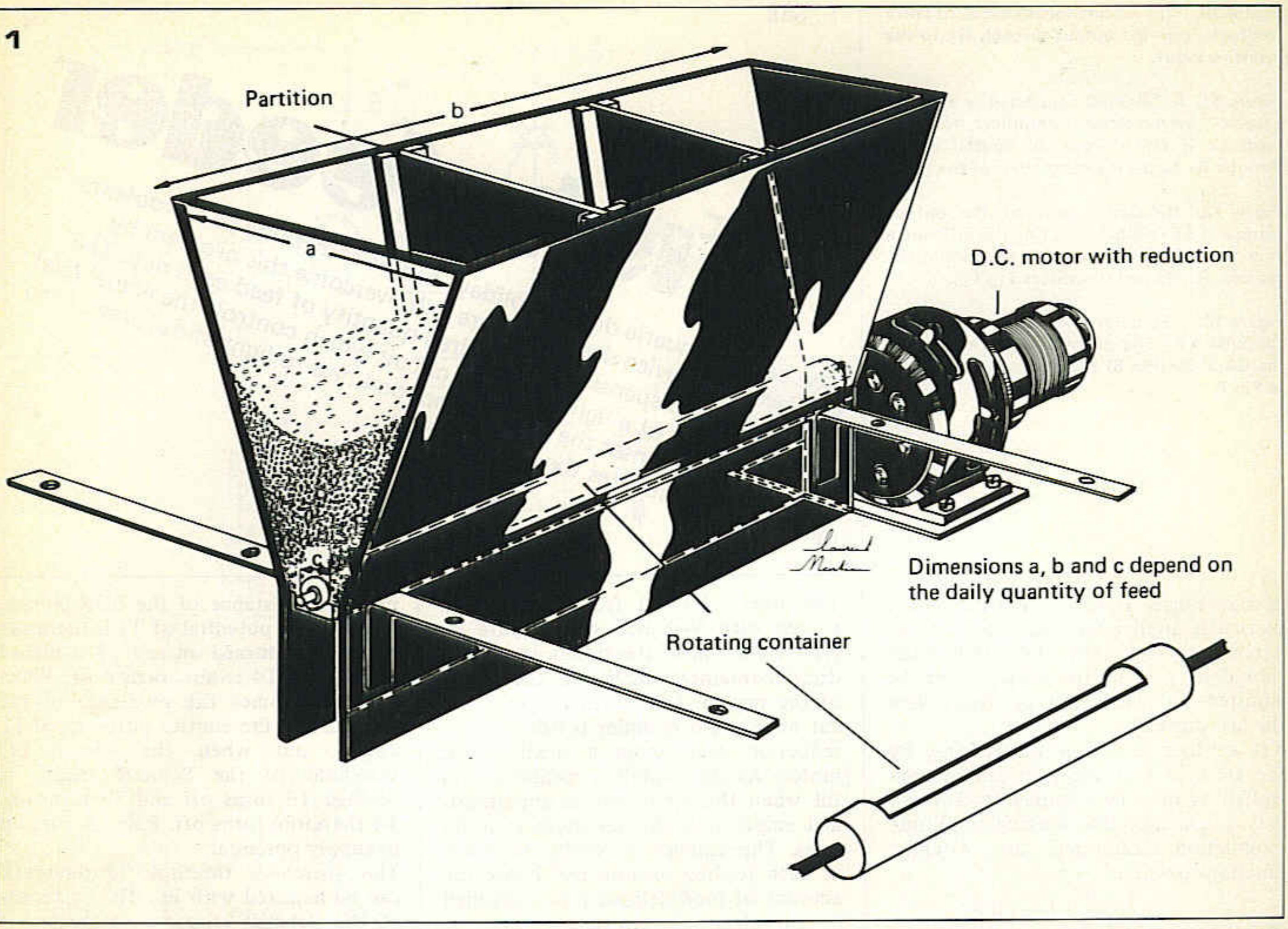


The switch-on threshold at daybreak can be adjusted with P1. The hysteresis of the Schmitt trigger is so great that even large brightness variations during the day will not cause spurious triggering. However, care must be taken to ensure that the LDR is screened from room lighting so that spurious triggering does not occur in the evening.

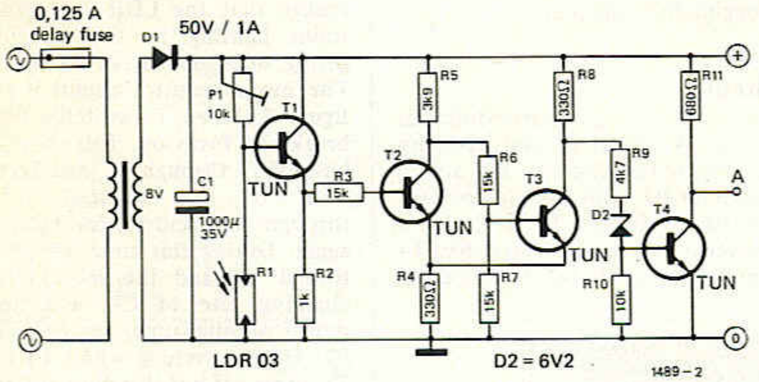
The motor control circuit is shown in figure 3. When T4 switches off at daybreak, T5 turns on. This shorts out the base of T6 through C2, and T6 turns off until C2 has charged sufficiently through R15 and P2 for T6 to turn on again. During this time T7 and T8 are turned on and the motor runs. The charging rate of C2, and hence the motor running time, can be adjusted by P2. In the evening when T4 turns on, T5 turns off but this does not affect the state of the following stage, so no feeding occurs.

If the fish feeder is to be used other than at holiday times the triac switch of figure 4 may be used to control the aquarium lighting. It is important to include C3 across the choke of the fluorescent tube to avoid high voltages being applied to the triac. If the lighting circuit is connected to the automatic feeder it is imperative to ensure that the finished construction is adequately insulated as the ground connection of the fish feeder is connected to the mains neutral. No part of the circuit should be accessible, and in particular the motor should be insulated, including the drive shaft. Potentiometer P2 should have a plastic shaft, and the whole assembly should be mounted in a plastic box, with no metal protrusions.

1


Partition
b
a
c
D.C. motor with reduction
Dimensions a, b and c depend on the daily quantity of feed
Rotating container

2



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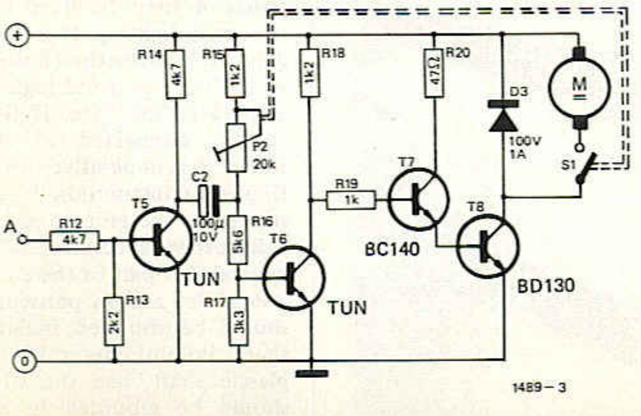

Construction of the dispenser

The dispenser is probably best constructed of clear acrylic sheet, so that the level of food may easily be seen. This may be glued together with acrylic cement. Motors with suitable reduction gearboxes can be obtained from most model shops.

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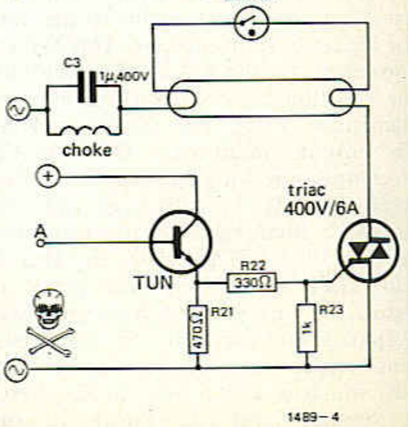
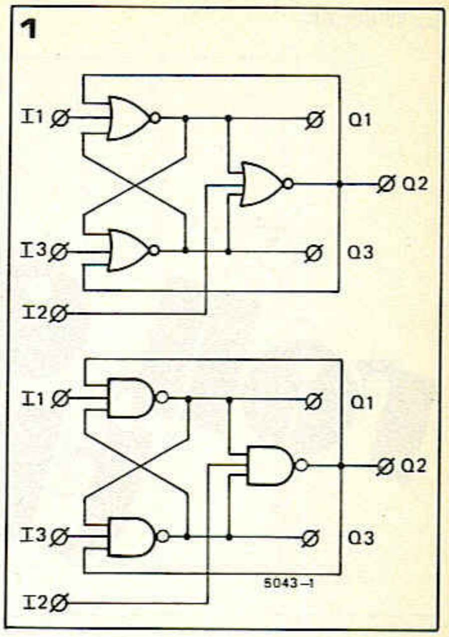


J. Koper

tri-stable

It is possible to use two NAND or NOR gates to make up a flipflop - a circuit with two stable conditions. The process can be extended to obtain circuits with three or even more stable states.

1



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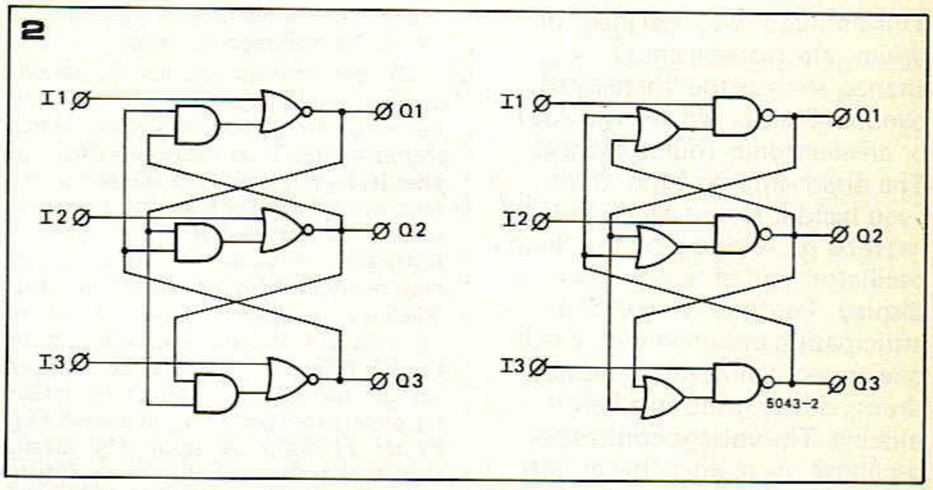

The arrangements shown in figure 1 both have 3 stable states. The state taken up by the outputs will depend on the input conditions applied. These circuits have the objection that correct operation is only guaranteed when drive is applied to two of the inputs at once (see table 1).

It is however possible to modify the circuits so that a single input drive will produce the desired output state. The circuit as a whole becomes more extensive; but it becomes easier to use. Figure 2 shows the modified arrangement. The operation of this circuit can be followed from table 2.

Figure 3 shows a master-slave shift register. If C is at logic '1', then the OR-gate outputs will also be '1', so that the state of Q_1-Q_2-Q_3 does not change. If C becomes '0', the AND-gate outputs will also be '0', so that the state of Q_4-Q_5-Q_6 is held.

Suppose for example that C is logic '0', with I_1 = '0', I_2 = '0' and I_3 = '1'. We find that Q_1 = '1', Q_2 = '1' and Q_3 = '0'. Since C is '0' the state of Q_4-Q_5-Q_6 is maintained. If C now goes to '1', the outputs Q_1, Q_2 and Q_3 will not change. This state is also the state at the inputs I_4, I_5 and I_6. Q_4 therefore becomes '0', Q_5 also '0' and Q_6 '1'. This shows that the input information '0'-'0'-'1' appears, after one clock pulse, at the output. ◾

NOR gates

I_1	I_2	I_3	Q_1	Q_2	Q_3
0	0	0	x	x	x
1	1	0	0	0	1
1	0	1	0	1	0
0	1	1	1	0	0
1	1	1	0	0	0

NAND gates

I_1	I_2	I_3	Q_1	Q_2	Q_3
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	1
1	0	0	0	1	1
1	1	1	x	x	x

Table 1

NOR gates

I_1	I_2	I_3	Q_1	Q_2	Q_3
0	0	0	x	x	x
1	0	0	0	1	1
0	1	0	1	0	1
0	0	1	1	1	0
1	1	1	0	0	0

NAND gates

I_1	I_2	I_3	Q_1	Q_2	Q_3
0	0	0	1	1	1
0	1	1	1	0	0
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	x	x	x

Table 2

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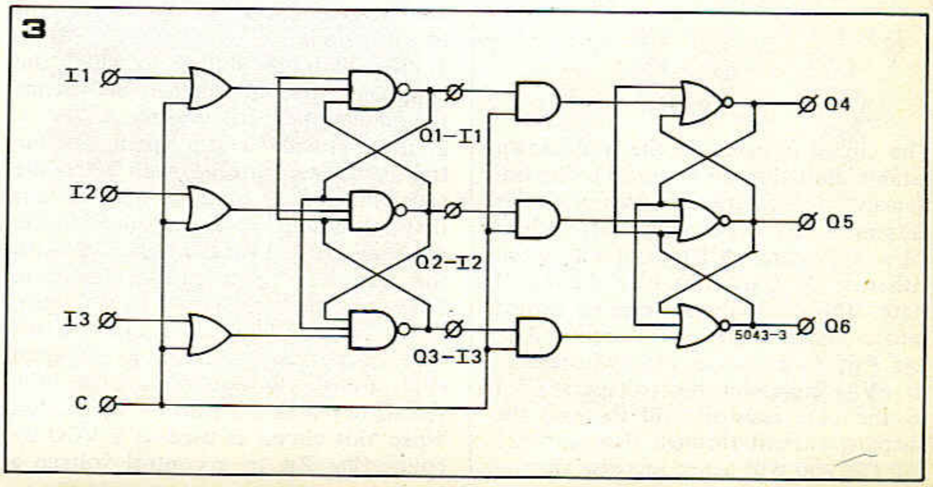

L. Wiechers

roll out the bandit

This oscillator was designed for driving electronic games of chance, such as the 'three-eyed bandit' (Elektor No. 2 page 238) or an electronic 'roulette wheel'. The disadvantage of the 'three-eyed bandit' is that a stop button must be pressed to stop the three oscillators and obtain the final display. Thus the tension and anticipation obtained with a real one-armed bandit as the number drums slowly grind to a halt is missing. The voltage-controlled oscillator overcomes this by providing an output whose frequency slowly reduces until it finally stops. This can also be used to simulate the 'rolling out' of the ball in a roulette wheel.

The circuit is based on the well-known astable multivibrator (figure 1). The frequency of oscillation of this circuit is determined by the charging current into C1 and C2 through R_{B2} and R_{B1} when either of the transistors is in the cutoff state. The multivibrator can be turned into a simple VCO by connecting R_{B1} and R_{B2} to a seperate supply instead of to $+V_b$. Increasing the voltage applied to the base resistors will increase the charging current through them into C1 and C2, and will hence increase the frequency of oscillation. Reducing the voltage has the opposite effect.

There are however, certain limitations to this simple approach. The base resistors perform two functions. When (for example) T1 is turned on R_{B1} supplies its base current. The minimum current must be such that the transistor remains in saturation. This places a restriction on the minimum voltage that may be applied for a given base resistor. When T1 is turned off and T2 is turned on, R_{B1} supplies the discharge current for C2 whilst R1 supplies the charging current for C1. For correct operation C1 must have charged up to almost $+V_b$ before T1 turns on again. This means that C2 must discharge more slowly than C1 charges, and this limits the maximum control voltage that may be applied to the base resistors. In practice frequency changes of between 10 : 1 and 50 :1 can be achieved, depending on the gain of the transistors. This is insufficient for this application.

Base current feed through zener diodes

The limited frequency range can be extended by the circuit of figure 2. Normally the coupling capacitors supply a portion of the base current whilst they are charging from the collector resistors, but this ceases as soon as the capacitors are charged. The zener diodes perform two functions:

1. they limit the voltage to which the coupling capacitors charge, and hence the time required for charging.
2. they provide a D.C. path for the transistor base current, even when the capacitors have charged. This means that the base resistors only provide the discharge current for the capacitors with the transistors in a cutoff condition. They can thus be much larger. Also, since one transistor is always cut off, only one base resistor is required (shown dotted in figure 2) provided the transistor bases are isolated by diodes. When this circuit is used as a VCO by connecting R_B to a control voltage a

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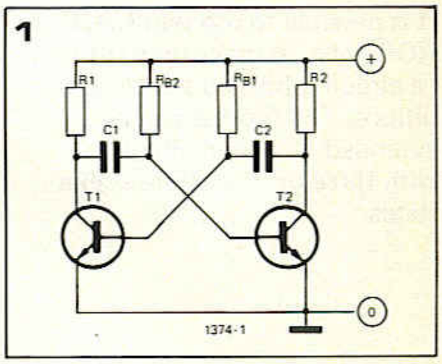

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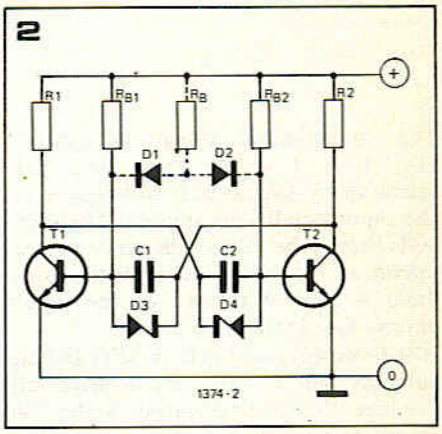

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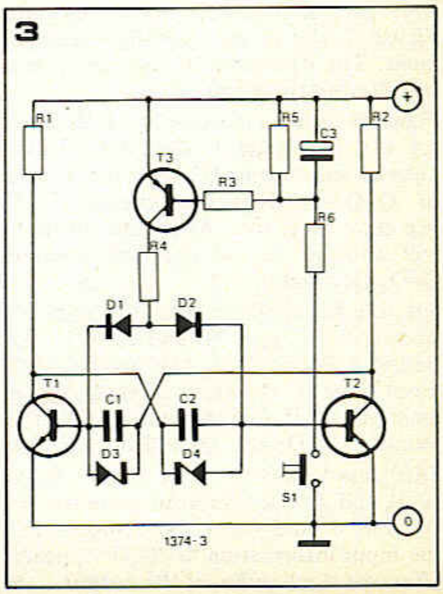


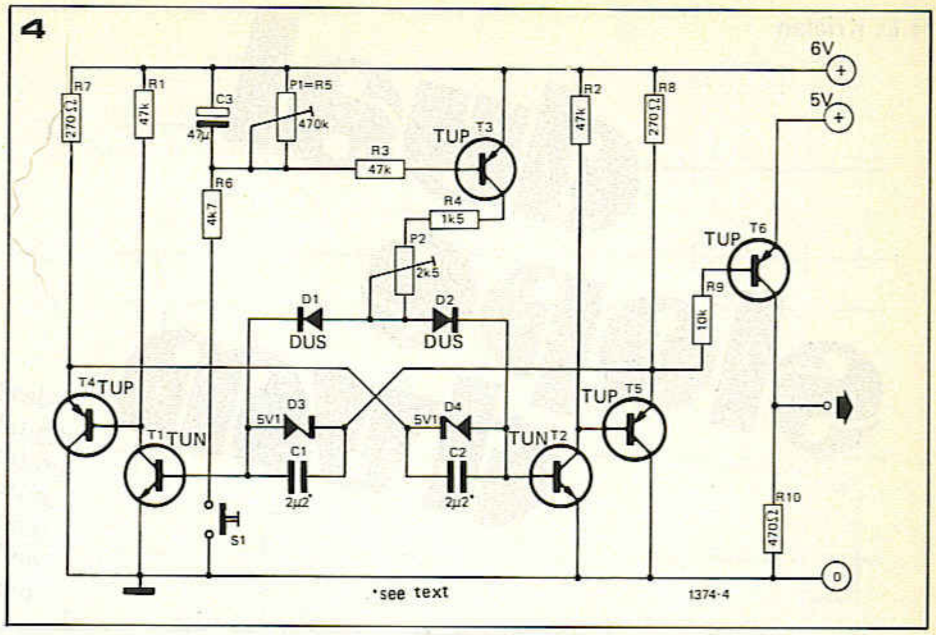
Figure 1. A basic astable multivibrator. This may be voltage-controlled by connecting the base resistors to a variable voltage instead of $+V_b$.

Figure 2. Addition of zener diodes makes transistor base current almost independent of base resistors. The two base resistors can be replaced by a single resistor and two diodes.

Figure 3. Base resistor replaced by a voltage-controlled current source.

Figure 4. Addition of emitter followers improves risetime without sacrificing loop gain. T6 further improves risetime and drives TTL.

4



frequency range of between 200 : 1 and 500 : 1 is obtainable.

Decaying frequency characteristic

The next step is to achieve the gradual decay of frequency required. This is accomplished in the circuit of figure 3. When the pushbutton is pressed C3 is charged rapidly. The voltage on C3 turns on T3 which causes the oscillator to start. As C3 slowly discharges the collector current of T3 decreases and the oscillator frequency reduces until the voltage across C3 is less than about 0.6 V, when T3 cuts off and the oscillator stops.

The final circuit

Figure 4 shows the final circuit. Emitter followers T4 and T5 are incorporated to provide a low impedance charging path for the coupling capacitors, thus improving the rise time of the waveform without reducing R1 and R2, which would reduce the loop gain. T6 converts the output to a level suitable for driving TTL circuits.

The discharge rate of C3, and hence the 'rolling out' time, is adjusted by P1. The initial frequency of oscillation is adjusted by P2. Note that C1 and C2 should be non-electrolytic types.

With the component values shown the results obtained were as follows:

Starting frequency 100 to 300 Hz.
Final frequency about 0.3 Hz.
'Rolling out' time 25 s maximum.

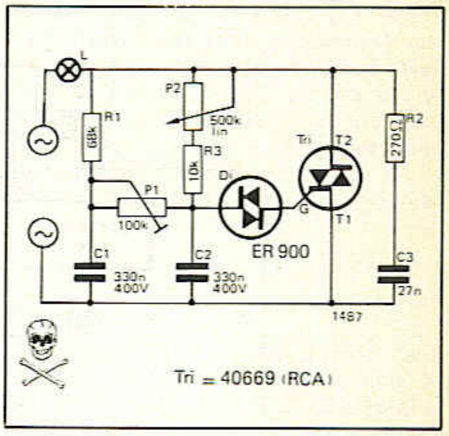
---

light dimmer

This simple triac dimmer can be used to control incandescent filament lamps up to 1500 W. The circuit operates on the phase-control principle. The main control is provided by P2. This determines the rate at which C2 charges and hence the point along the mains waveform at which the voltage on C2 reaches the breakdown voltage of the diac, which is when the triac is triggered. P1, in conjunction with R1 and C1 determines the minimum brightness level, or alternatively may be used as a fine brightness control. Interference suppression is provided by R2 and C3.

Construction

The printed circuit board is very compact and can easily be accommodated inside the modern, square type of flush-mounting switch panel, or in a small box for portable applications. The following safety points should be noted. No part of the circuit should be accessible from the outside. The case should preferably be made of plastic or other insulating material, and fixing screws for the board should be nylon. If a metal case is used the board must be adequately insulated from it and the case should be earthed. The potentiometer should have a plastic spindle.



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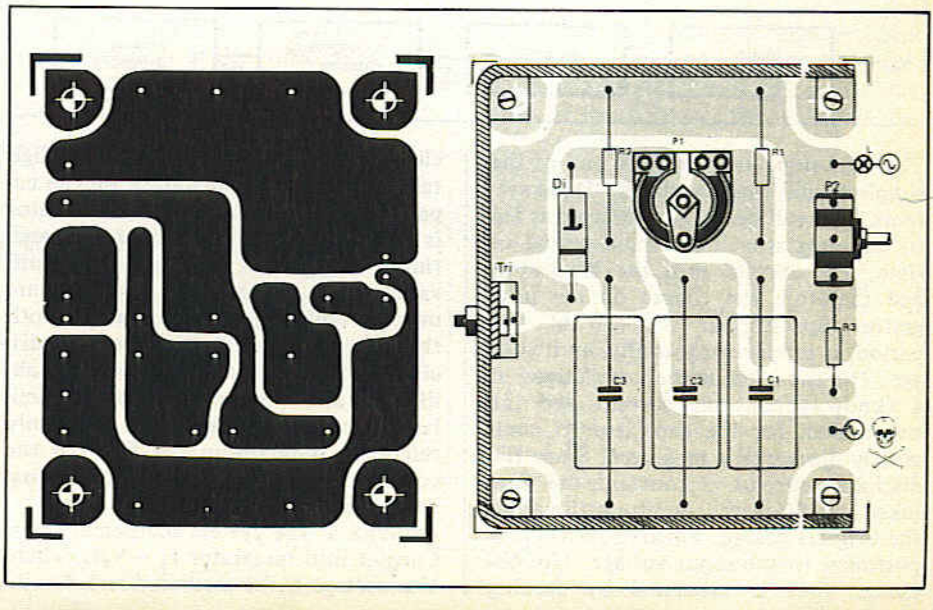

H.L. Krielen

dual slope dvm

A design is described here for a basic 2½ digit digital voltmeter using the dual-slope integration principle. The DVM has a full-scale sensitivity of 199 mV, but may be extended at the constructor's option with multiplier resistors and shunts to measure other voltages and current.

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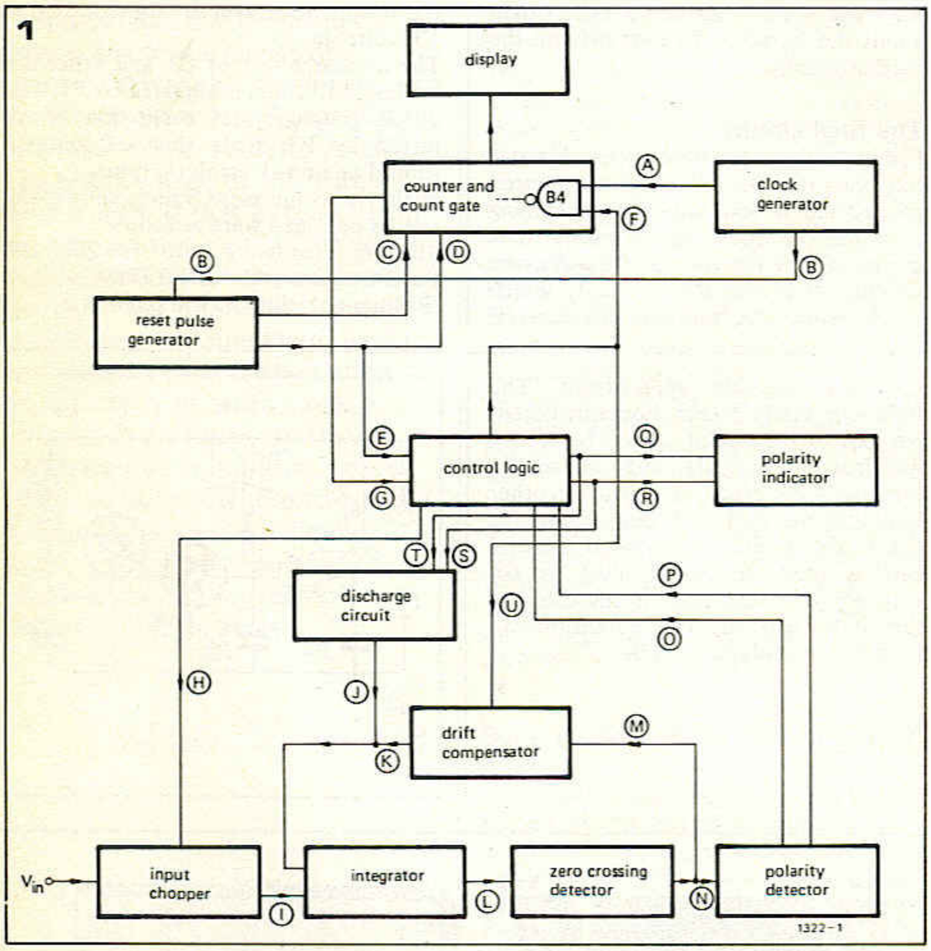


Figure 1. Block diagram of the complete DVM. The arrows in the various connections indicate the direction of action.

Figure 2. The input voltage applied.

Figure 3. The time axis. The time t_1-t_2 is the charging time, t_2-t_3 is the discharge time, and t_3-t_0 is the display time.

Figure 4. Output voltage of the reset pulse generator.

Figure 5. The input voltage to the integrator.

Figure 6. The discharge current of the integrator.

Figure 7. The output voltage of the integrator.

Figure 8. The output voltage of the zero-crossing detector.

Figure 9. The clock pulses applied to the counter. They first consist of 100 reference pulses, which determine the charging time, followed by a number of pulses proportional to the voltage of the input signal. The frequency of these pulses can be assumed to be constant during the time t_1-t_3.

Figure 10. The clock generator. Via line A the pulses go to the count gate, whilst via line B the reset pulse generator is driven.

Figure 11. The reset pulse generator. This supplies reset pulses to the counter (via C and D), and a start pulse to the control logic (via E).

The dual-slope technique is one of the simplest and most reliable DVM systems. The voltage to be measured is fed to an integrator for a fixed period of time. The current into the integrator, and therefore the charge on the integrator capacitor at the end of this period, is proportional to the input voltage. The capacitor is then discharged at a (known) constant current and the time taken for the capacitor to completely discharge is measured. Since the discharge current is constant the time taken to discharge is proportional to the original charge, which in turn is proportional to the input voltage. The discharge time is measured by feeding clock pulses from an oscillator to a digital counter until the voltage on the capacitor reaches zero. The same oscillator is used to determine the original charge time. This means that any long-term variations in the oscillator frequency are unimportant since they will affect both the charge time and the measured discharge time equally. The long-term stability and absolute frequency of the oscillator are thus unimportant. The only reference standard in the DVM is the constant discharge current, which must be stable.

Looking at the system mathematically: Current into integrator $I_1 = V/R$, where V is voltage to be measured and R is integrator input resistor.

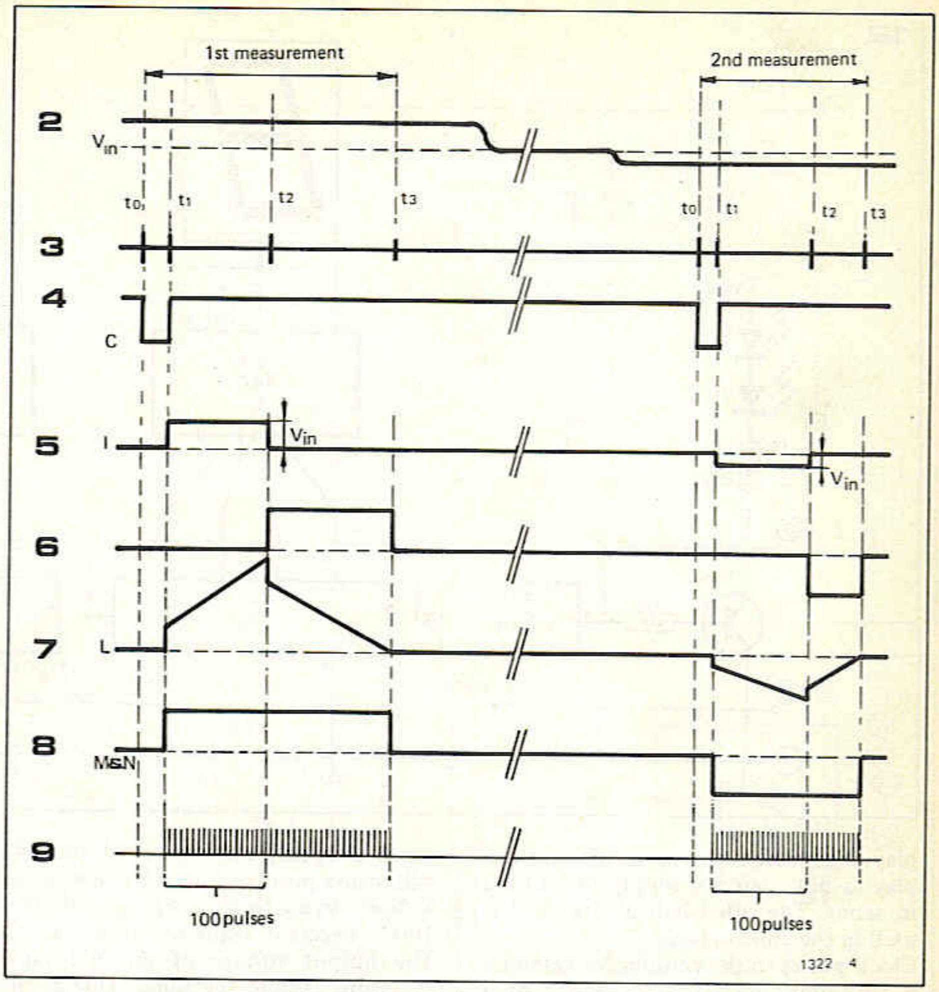
Charge on integrator capacitor at end of charge period Δt_1

$$Q = I_1 \Delta t_1 = \frac{V}{R} \cdot \Delta t_1 :$$

Time taken for capacitor to discharge at constant current I_2

$$\Delta t_2 = \frac{Q}{I_2} = \frac{V \Delta t_1}{I_2 R}.$$

Since Δt_1 and Δt_2 are derived from the same oscillator it can be seen that a variation in oscillator frequency will affect both Δt_1 and Δt_2 equally, and the final result will remain the same, provided I_2 does not change and R is fixed.



The block diagram of the DVM is given in figure 1 and an operational timing diagram in figures 2-9. The timing diagram is drawn for both a positive and a negative input voltage.

The sequence of operation is as follows: the input chopper applies the input voltage (figure 2) to the integrator for a fixed time t_1-t_2 (figure 3). The chopped input to the integrator is shown in figure 5. During this time the integrator output rises linearly as the capacitor charges (figure 7). The step in the integrator output waveform at the beginning and end of the charge period is explained in the detailed description of the integrator later in the text.

At the end of the charge period the integrator is disconnected from the input voltage and is connected to the discharge circuit. The integrator capacitor discharges linearly during the period t_2-t_3 (figure 6). During the whole period t_1-t_3 the output of the zero-crossing detector (figure 8) is positive. When the voltage on the integrator capacitor reaches zero the output of the zero-crossing detector falls to zero. This is used to control the clock pulses to the counter (figure 9). The operation is effected by the control logic in the block diagram. Before each measuring period the counter and control logic are reset by a pulse from the reset oscillator (figure 4).

Measurement of a negative voltage is performed in a similar manner. The only differences are that the output of the zero-crossing detector is negative. This is detected by the polarity detector and is used to reverse the polarity of the constant current from the discharge circuit. (Otherwise the integrator output, being already negative, would simply become more negative and would never cross zero.)

A refinement is incorporated in the form of a drift compensator circuit, which nulls out the effect of zero drift in the integrator and zero-crossing detector.

Circuits in the DVM

Clock Generator

The clock generator, which provides drive pulses for the counter, is shown in figure 10 and consists simply of a two-transistor astable multivibrator with a frequency of approximately 15 kHz. As stated earlier, the long-term stability of this oscillator is unimportant.

The Reset Pulse Generator

This circuit is shown in figure 11 and is based on a programmable unijunction transistor, T14. The gate of this device receives a D.C. bias from R42 and R43. Pulses from the clock generator are applied to point (B) and charge up C7 through D10 and R41. When the unijunction fires C7 discharges through the unijunction and R44, and the voltage across R44 causes T10 to turn on. This causes T11 to turn off. A negative-going pulse is therefore available at the collector of T10 and a positive-going pulse is available at the collector of T11. The time between reset pulses is determined by the time constant R41 x C7, and in this case is one second. The interval between reset pulses determines the measurement repetition rate and also the time for which each reading is displayed. It may be altered to suit personal taste, provided it is longer than the measuring period t_1-t_3.

C7 should be a low-leakage type, preferably tantalum.

The Counter

The counter circuit (figure 12) consists of two 7490 decade counters and a JK flipflop (half of a 7473). The 7490's count the two least significant decades and drive 7447 seven segment decoders and LED or Minitron displays. The JK flipflop counts the 'hundreds'. Since the maximum display is 199 only a one need be displayed by the hundreds dis-

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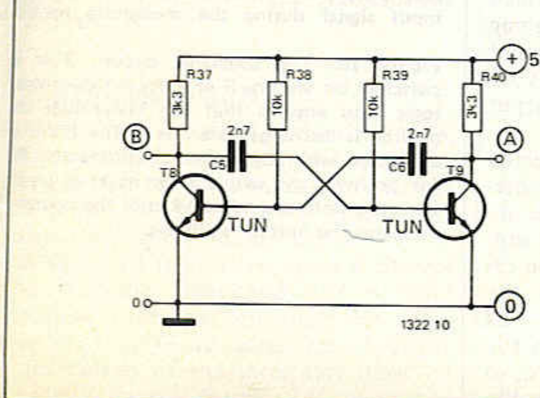

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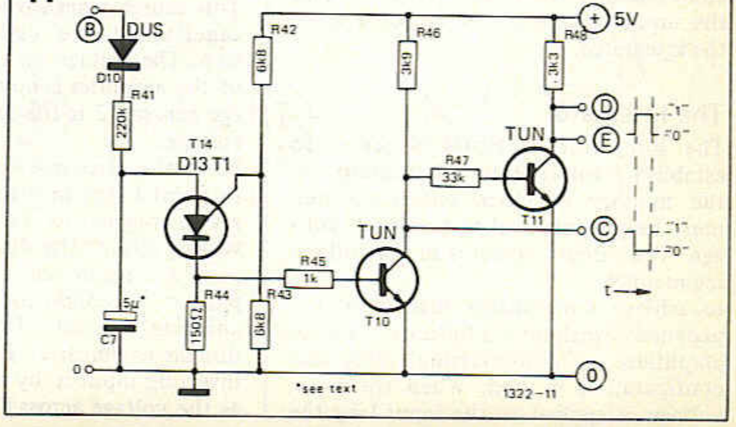

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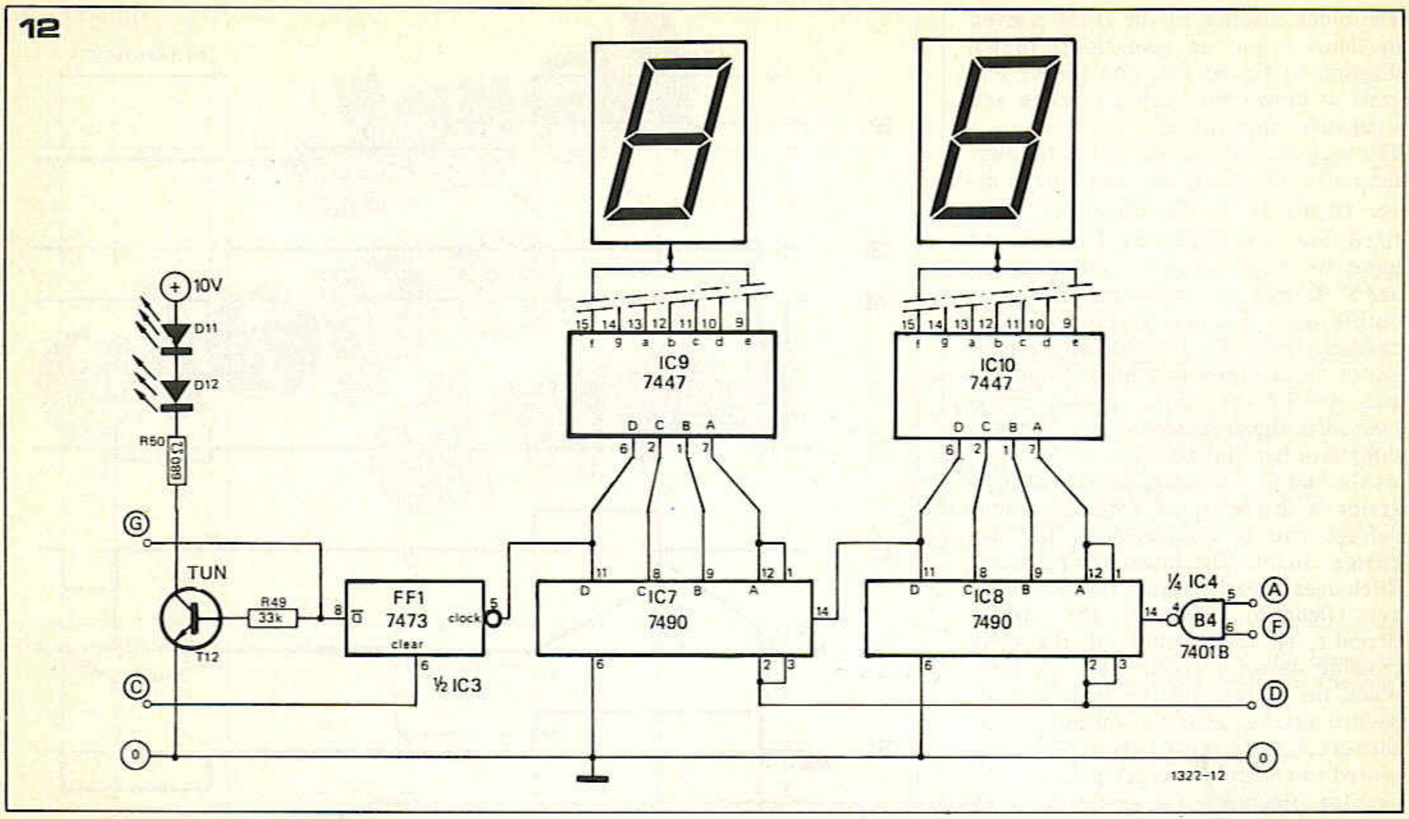

Figure 12. The counter. C and D are reset inputs, A is the count input, F the driver for the count gate. Output G supplies a pulse to the control logic at the one hundredth count pulse.

Figure 13. The input chopper. It is driven via line H, and during the time t_1-t_2 it passes the input signal on to the integrator (via line I).

Figure 14. The integrator. I is the input and L the output. The lines J and K, come from the discharge circuit and the drift compensator, respectively. C2 is the integration capacitor. P1 serves for zero-adjustment: with input I to earth and the lines J and K interrupted, the output L must be adjusted to 0 with this potentiometer.

Figure 15. The zero-crossing detector. It amplifies the output voltage of the integrator (line L), and drives the drift compensator and the polarity detector (via M and N).

Figure 16. The polarity detector. This is in fact a three-position switch: for input voltages higher than +600 mV output 0 is 'low' and P 'high'; for voltages between +600 mV and −600 mV both outputs are 'high'; whilst for voltages below −600 mV 0 is high and P is low.

Figure 17. The polarity indicator. It drives the pilot lamps, depending on the polarity of the input signal during the measuring period.

Figure 18. The discharge circuit. This is switched on via line S or T from the control logic, and ensures that the integration capacitor is discharged via line J. The DVM is calibrated with adjustment potentiometer P2 for positive, and with P3 for negative input voltages. Both are adjusted until the counter indicates one unit per millivolt.

play. For economy, a seven segment display is not used but simply two LED's in series. The other half of the 7473 is used in the control logic.
Clock pulses to the counter are gated by a two-input NAND-gate (quarter of a 7401).

Input Chopper

The input chopper (figure 13) connects the input voltage to the non-inverting input of the integrator during the charge period, t_1-t_2. For the rest of the measurement cycle it grounds this input. The circuit functions as follows:
during the interval t_1-t_2 point H is at logic '1' (+5 V) so T1 is turned off. T2 is also turned off. The gate of F1 is held at about −10 V so F1 is cut off. The gate of F2 is held at about −1.2 V, so F2 is turned on. The input voltage therefore appears at point I via the FET F2, and is thus fed to the input of the integrator.
At time t_2 point H becomes low, so T1 and T2 are both turned on. The gate voltage of F1 becomes about −2 V, so it conducts and grounds the input of the integrator. The gate voltage of F2 becomes about −10 V, so it is cut off and the input voltage is disconnected from the integrator.

The Integrator

The integrator of figure 14 serves to establish a voltage-time relationship, i.e. the number of clock pulses counted must be proportional to the input voltage. The circuit operates in the following manner:
to achieve a reasonably high input impedance without additional buffer amplifiers a non-inverting integrator configuration is used. When the input voltage is applied to the input I by the input chopper, the output of the 741 will swing positive. Since C2 appears as a short circuit to this step input there is 100% negative feedback through C2. The output voltage of the 741 must therefore assume the same value as the voltage on the inverting input (pin 4), which by definition is the same as the input voltage on pin 5. The input voltage thus appears at the output as a positive-going step. Since there is now a voltage across R12 a (constant) current flows through it which is proportional to the input voltage. Since no current can flow into the inverting input of the 741 this current must flow into C2. Since the current is constant the charge on the capacitor, and therefore the voltage across it, increases linearly. The capacitor is allowed to charge for a period of 100 clock pulses. The voltage across C2 is then

$$V = \frac{I_1 \cdot \Delta t}{C_2} = \frac{V_{in} \cdot \Delta t}{R_{12} \cdot C_2}$$

where Δt represents the time interval t_1-t_2.
At time t_2 the input chopper disconnects the input voltage and grounds the non-inverting input of the integrator. This causes a negative-going step, which cancels out the earlier positive-going step. The voltage on the inverting input of the amplifier is now zero, so the voltage across C2 is the same as the output voltage.
When the discharge circuit is connected to point J (the inverting input) the integrator begins to function in the inverting mode. The discharge circuit supplies a constant current I_2 into the capacitor of opposite polarity to the charging current. The capacitor thus discharges linearly. The voltage on the inverting input is, by definition, zero, so as the voltage across C2 falls so does the

741 output voltage (which is identical). During this time the counter is counting clock pulses, until the zero-crossing detector monitors zero volts on the output of the 741. The discharge time Δt_X is given by: voltage on C2,

$$V = \frac{I_1 \cdot \Delta t}{C_2} = \frac{I_2 \cdot \Delta t_X}{C_2}$$

therefore

$$\Delta t_X = \frac{I_1 \cdot \Delta t}{I_2}$$

but

$$I_1 = \frac{V_{in}}{R_{12}}$$

therefore

$$\Delta t_X = \frac{V_{in} \cdot \Delta t}{R_{12} I_2}$$

Since Δt, R12 and I_2 are all fixed Δt_X is proportional to V_{in}.

The Zero-Crossing Detector

This circuit also uses an op-amp (figure 15), but in this case a 709 is used which has a greater slew-rate than the 741. The circuit has a high gain, about 70 x, so a small swing of the input voltage positive or negative will make the output swing hard over to plus or minus 10 V. D5 and D6 provide input protection by limiting the voltage on pin 5 of the IC to about ±0.2 V maximum, and R23 limits the current through the diodes. C3 and C4 are included to keep the 709 stable.

The output of the zero-crossing detector is connected to the input of the polarity detector (figure 16). For outputs from the zero-crossing detector greater than +0.6 V T6 is turned on and T7 is turned off, while for outputs more negative than −0.6 V T7 is turned on and T6 is turned off. For voltages between −0.6 V and +0.6 V both transistors are turned off, thus providing a zero indication.

Polarity Indicator

This consists of two high power NAND-gates (7440), connected as a set-reset flipflop (figure 17). During the measuring period this flipflop is either set or reset by the polarity detector depending on the polarity of the measured voltage and the appropriate LED is lit. The flipflop is necessary to store the polarity indication during the display period, when the output of the integrator (and hence of the zero-crossing detector) is zero.

The Discharge Circuit

There are in fact two discharge circuits, one of which is used depending on the polarity of the input signal. The circuit is shown in figure 18. When the input signal is positive, the output of the 741 in figure 14 is positive, and C2 charges so that the 'right-hand' end is more positive than the 'left-hand' end. This means that to discharge the capacitor the output of the integrator must be negative-going during the discharge

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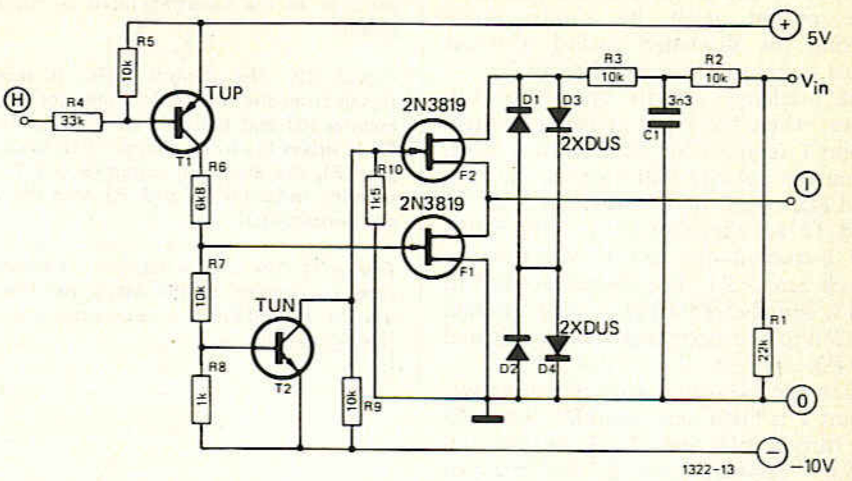

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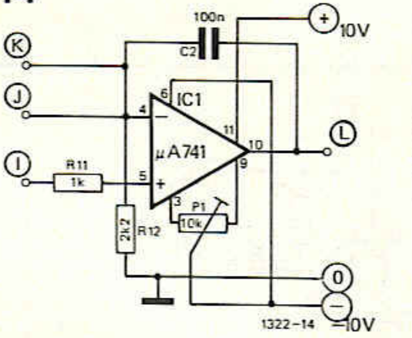

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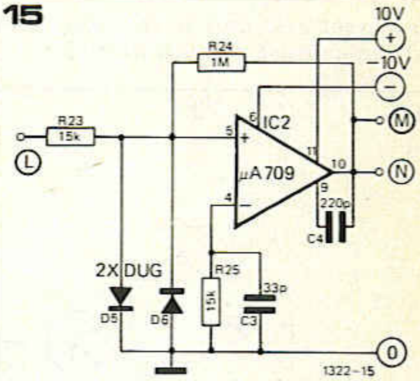

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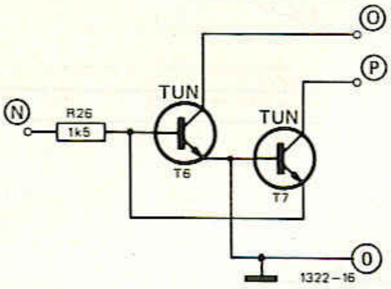

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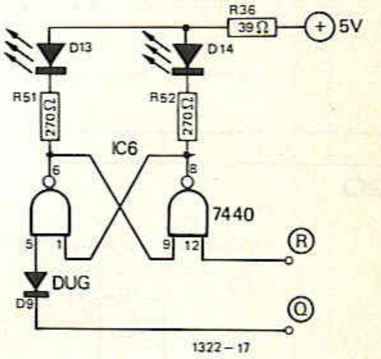

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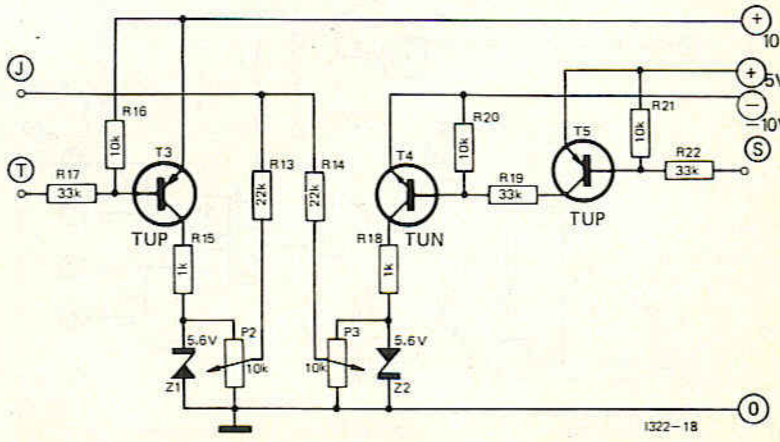

period. Current must therefore flow into point J. For a negative input signal the output of the integrator is negative, so the output must be positive-going during the discharge period. Current must therefore flow out of point J.
The discharge circuits operate as follows: when the input signal is positive point T is grounded by a control signal from the polarity indicator via the control logic while point S remains high. T4 and T5 are therefore turned off, whilst T3 is turned on. +5.6 V therefore appears across Z1. The voltage applied to R13, and therefore the current through R13 into the integrator, can be adjusted by P2.
When the measured voltage is negative, point T is 'high' and point S is 'low'. T3 is turned off and T4 is turned on. −5.6 V appears across Z2 and the current through R14 can be adjusted by P3.

The Drift Compensator

To prevent zero drift in the integrator and zero-crossing detector from causing inaccuracies feedback is applied round these circuits during the display period. During this time point U is low, so T13 is turned on and hence F3 is conducting (figure 19). Points M and K are connected to the output of the zero-crossing detector and the inverting input of the integrator respectively, so any voltage offset on the output of the zero-crossing detector will be integrated, which will tend to null out the offset.
During the measuring period point U is 'high', and the drift compensator is switched off so that the integrator and zero-crossing detector can function normally.

Figure 19. The drift compensator. It is switched on via line U, and provides a feedback from the output of the zero-crossing detector to the inverting input of the integrator.

Figure 20. The control logic. It receives signals from the reset pulse generator (E), the counter (G) and the polarity detector (0 and P). It drives the input chopper (H), the count gate (F), the discharge circuit (S and T), the polarity indicator (Q and R) and the drift compensator (U).

Figure 21. The overall diagram. P1 serves for zero adjustment of the integrator (see figure 14). P2 and P3 serve to calibrate the DVM (see figure 18).

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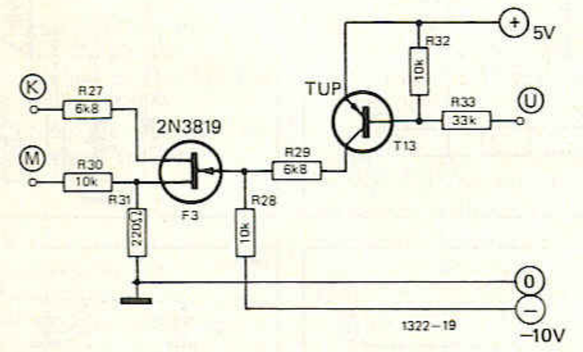

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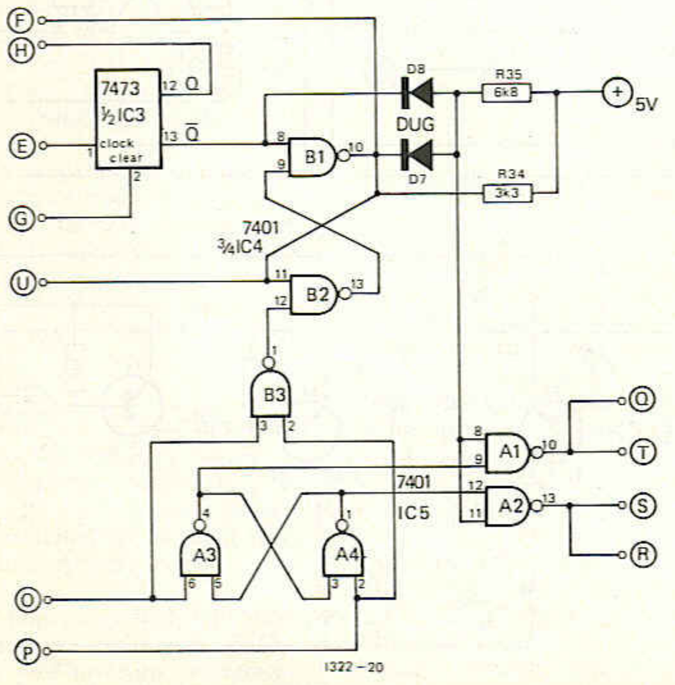

Control logic

The measurement sequence timing is performed by the control logic, the circuit of which is given in figure 20. The measurement sequence starts with a positive pulse from the reset pulse generator, which resets the counter via point D (figure 12). This pulse is also applied to point E of the control logic, and on the trailing edge of the pulse the JK flipflop (½IC3) is set. The Q output connected to line H switches on the input chopper, whilst the $\overline{Q}$ output goes 'low' and sets the set-reset flipflop consisting of two NAND-gates. Output F thus goes 'high', opening the gate to the counter, so that it begins to count clock pulses. The drift compensator is also switched off via line U. A negative going pulse presets FF1 in figure 12 via line C. The $\overline{Q}$ output of the 7473 holds the inputs of gates A_1 and A_2 low via D8, which holds both inputs to the discharge circuit (S and T) high. The discharge circuit is therefore inoperative.
When 100 clock pulses have been counted (time t_2) output G in figure 12 goes 'low', resetting the JK flipflop (½IC3). The input chopper is now switched off via line H. In the meantime the flipflop comprising A_3 and A_4 has been either set or reset by the polarity detector. Since the $\overline{Q}$ output of the 7473 is now 'high' the outputs of A_3 and A_4 can be gated through A_1 and A_2 to set the polarity indicator via lines Q and R, and also to enable the appropriate part of the discharge circuit. The counter continues to count clock pulses. Note that it is not necessary to reset the counter at time t_2, as at the hundredth pulse it has reached zero!
When the output of the integrator reaches zero the output of the zero-crossing detector is also zero. Both outputs of the polarity detector go 'high', so the output of gate B_3 goes low, resetting the flipflop (B_1 and B_2), which disables the discharge circuit via D7 and A_1, A_2. The counter gate is closed via line F so the count ceases. The display now indicates the measured value of the input voltage until the next reset pulse.

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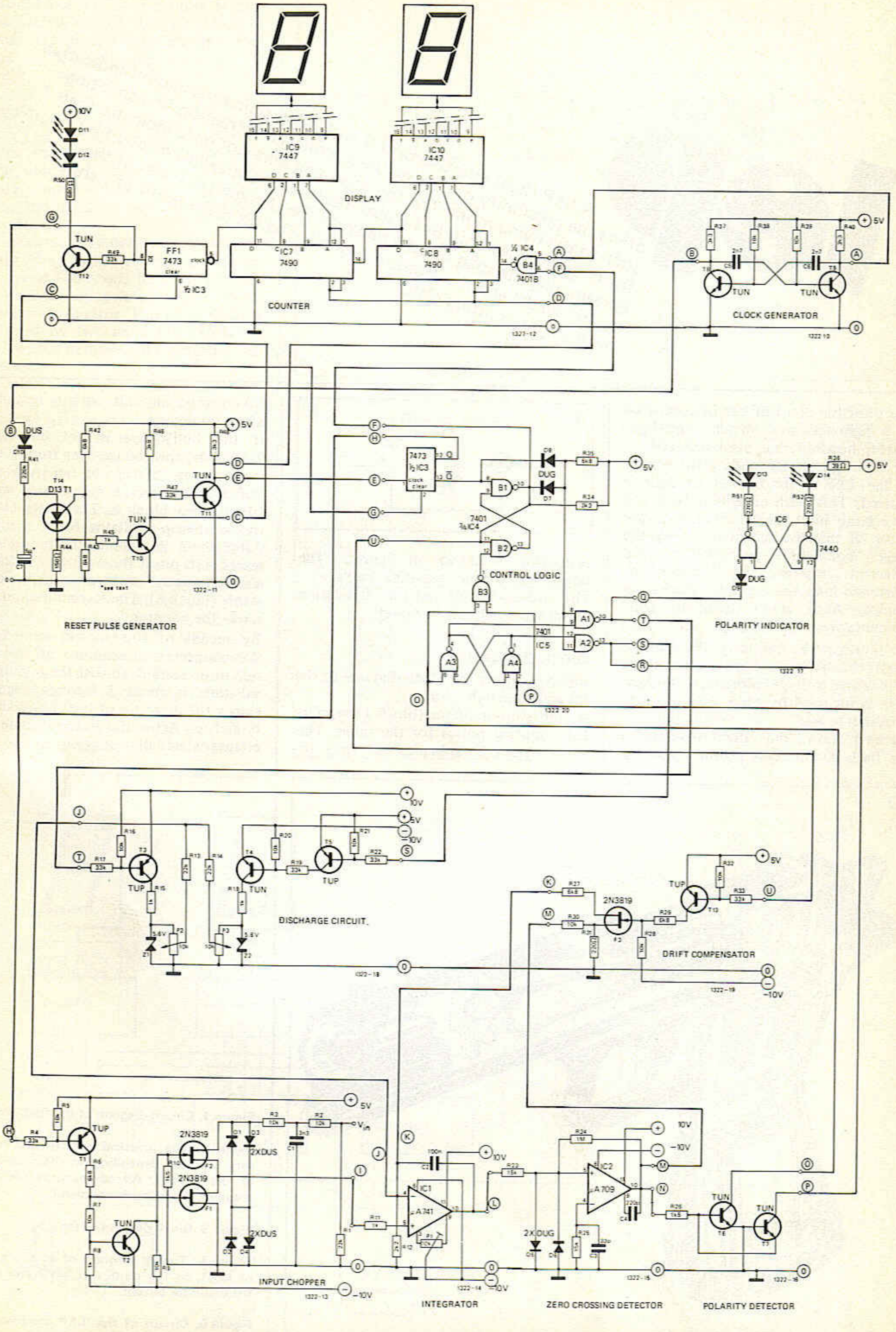
DISPLAY
IC9
7447
IC10
7447
COUNTER
IC7
7490
IC8
7490
FF1
7473
clock
clear
½ IC3
½ IC4
B4
7401B
+10V
D11
D12
R50
680Ω
TUN
T12
R49
33k
CLOCK GENERATOR
+5V
R37
R38
R39
R40
C5
2n7
C6
2n7
T8
T9
TUN
RESET PULSE GENERATOR
DUS
D10
R41
220k
D13 T1
T14
C7
R42
R44
R43
R45
R46
R47
33k
R48
T10
T11
*see text
CONTROL LOGIC
7473
½ IC3
7401
¾ IC4
B1
B2
B3
D8
D7
DUG
R35
R34
7401
IC5
A1
A2
A3
A4
POLARITY INDICATOR
D13
D14
R36
39Ω
R51
R52
IC6
7440
D9
DUG
DISCHARGE CIRCUIT
+10V
+5V
−10V
R16
R17
33k
T3
TUP
R15
R13
R14
5.6V
Z1
P2
10k
P3
10k
Z2
T4
TUN
R18
R20
R19
33k
T5
TUP
R21
R22
33k
DRIFT COMPENSATOR
R27
R30
R31
2N3819
F3
R28
R29
T13
TUP
R32
R33
−10V
INPUT CHOPPER
R5
R4
33k
T1
TUP
R6
R7
R8
T2
TUN
2N3819
F2
F1
R10
R9
D1
D2
2XDUS
D3
D4
2XDUS
R3
10k
R2
10k
C1
2n2
Vin
R1
−10V
INTEGRATOR
C2
100n
IC1
μA741
R11
R12
P1
R23
+10V
−10V
ZERO CROSSING DETECTOR
R24
1M
IC2
μA709
C4
C3
R25
2XDUG
D5
D6
+10V
−10V
POLARITY DETECTOR
R26
1k5
T6
TUN
T7
TUN
1322-12
1322-10
1322-11
1322-17
1322-20
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1322-19
1322-13
1322-14
1322-15
1322-16

A. Schulz

lep

A LEP (light emitting pistol) with electronic time and hit indication offers the possibility of moving the age-old fair attraction 'the shooting stall' to the living-room. The toy described here not only indicates that the target has been hit, but it also measures the speed of reaction by determining the span of time between the changing to green of the 'traffic lights' and the moment of a hit. The hit is the result of a shot from a light-emitting pistol.

The principle of a LEP can be compared to a light-activated switch. The light source, however, has been replaced by the light pistol. By pulling the trigger of the LEP a short flash of light is emitted. This flash of light is produced by a lamp built into the barrel of the pistol. A microswitch operated by the trigger, connects a previously charged capacitor across the lamp. Via this low-resistance load the capacitor discharges quickly. As a result the lamp lights momentarily.

To increase the intensity the lamp is briefly loaded with three to four times its nominal voltage. Moreover, the light flash is focussed by a biconvex lens into a parallel beam.

Figure 1 shows the circuit diagram of the flash circuit. One possible practical realisation is shown in figure 2. The target has a light sensitive bull's eye. The circuits for hit and time indication are situated behind the target.

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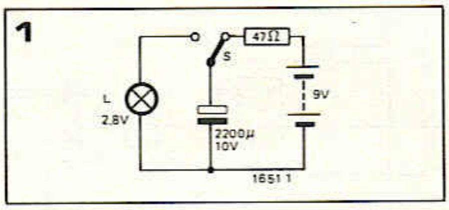

Block diagram

Figure 3 shows the block diagram of the hit and time indicator.

A start-stop-oscillator (block 1) supplies the counting pulses for the timer. This timer (block 2) indicates the time between start and hit with a resolution of 1/100 second.

If the bull's eye is not hit within 9 seconds, the change-over from 8 to 9 is used by means of an AND-gate (block 3) to start a monostable multivibrator via block 4. The latter blocks the start-stop-oscillator for 2 seconds. After these 2 seconds the monostable resets. As a result the oscillator is started simultaneously with a second monostable (block 6). The second monostable resets the counter.

By means of this second monostable the counter is maintained at zero for one more second, so that the total interval time is about 3 seconds. Figure 4 shows the diagrams of the pulse trains a, b and c. After this interval time the counter starts all over again.

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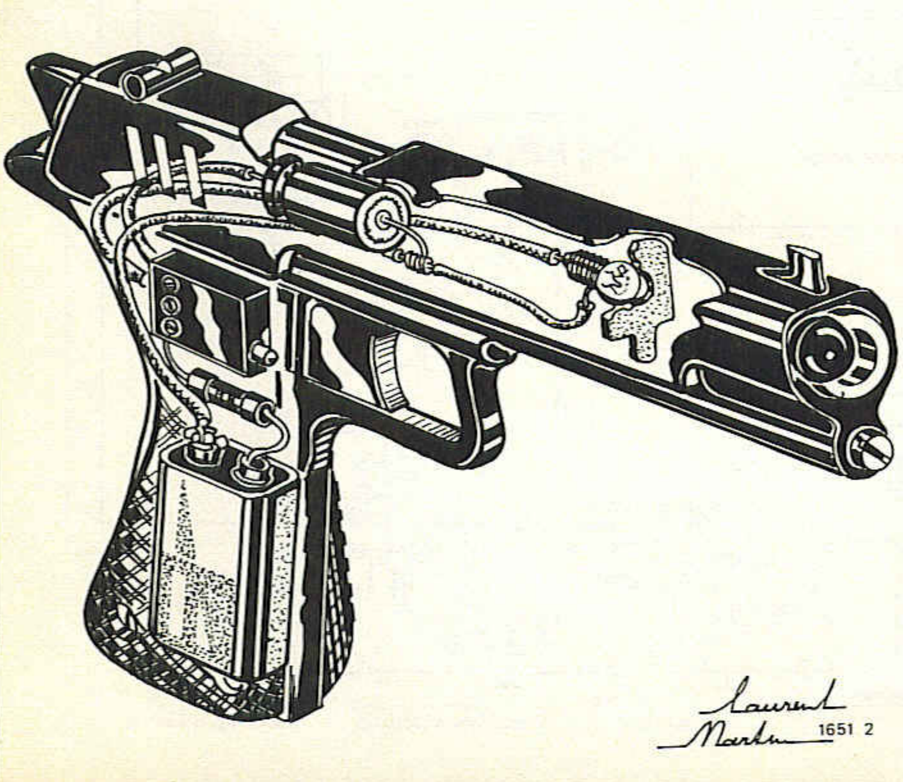

Figure 1. Circuit diagram of the flash circuit.

Figure 2. The practical construction can be very realistic, depending on the imagination of the builder. All components are easily accommodated inside the pistol.

Figure 3. Block diagram of the LEP.

Figure 4. Timing diagram of a: the output of MM1, b: the output of MM2 and c: the the oscillator output.

Figure 5. Circuit of the 'LEP complete with timer and traffic light'.

This counting cycle can be interrupted only by a direct hit on the light sensitive resistor (block 7). Then a pulse is produced which via the OR-gate (block 4) triggers the monostable multivibrator (block 5) so that the oscillator is stopped.

Diagram

Figure 5 gives the overall diagram of the hit and time indication. The indication unit uses three cascaded 7490 decade counters with 7447 decoders driving Minitrons and needs little further discussion.

The minitron has been chosen for the display. Any other seven-segment display could, however, be used instead. The counter input is connected to an astable multivibrator. This multivibrator is formed by two nand gates (N5 and N6) with frequency-determining elements.

A control unit starts and stops the oscillator, also resets the counter. An important part of the control unit is the hit detector built around T1.

Transistor T1 is adjusted so that it is normally conducting. The voltage divider consisting of R1 and R2 coupled by a capacitor can, however, briefly influence the bias of T1. When a light flash hits R2, the base of T1 will be briefly grounded. As a result T1 blocks and by means of the trigger circuit consisting of N1 and N2, a short pulse going from '1' to '0' is generated. This pulse is fed to a NAND (N4) which triggers the monostable multivibrator MM1 connected behind. The sensitivity of the trigger circuit can to some extent be adjusted with P1.

NAND N4 is used as an OR-gate here! As long as the output of the Schmitt trigger produces no pulse, it remains at the logic '1' level. The same applies to the output of N3. This output remains '1' until the last counter has reached position 1001. This happens after 9 seconds. As soon as the position 1001 is reached, the output of N3 changes to '0', so that MM1 is triggered via N4. From then on it is impossible to trigger MM1 from the hit indicator.

The triggering of the monostable multivibrator MM1 causes the oscillator formed by the gates N5 and N6 to be blocked, because one input of N6 is connected to the Q̄-output of MM1.

At the same time the set-reset flipflop (N7 plus N8) is reset by the Q̄-signal on the input of N8. As a result the output of N8 becomes '1' so that the red lamp, connected in the collector circuit of T2,

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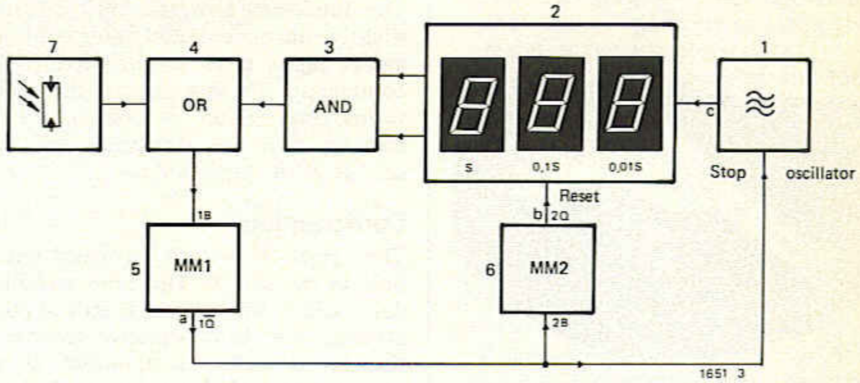

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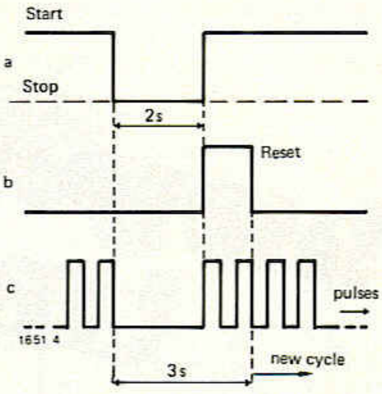

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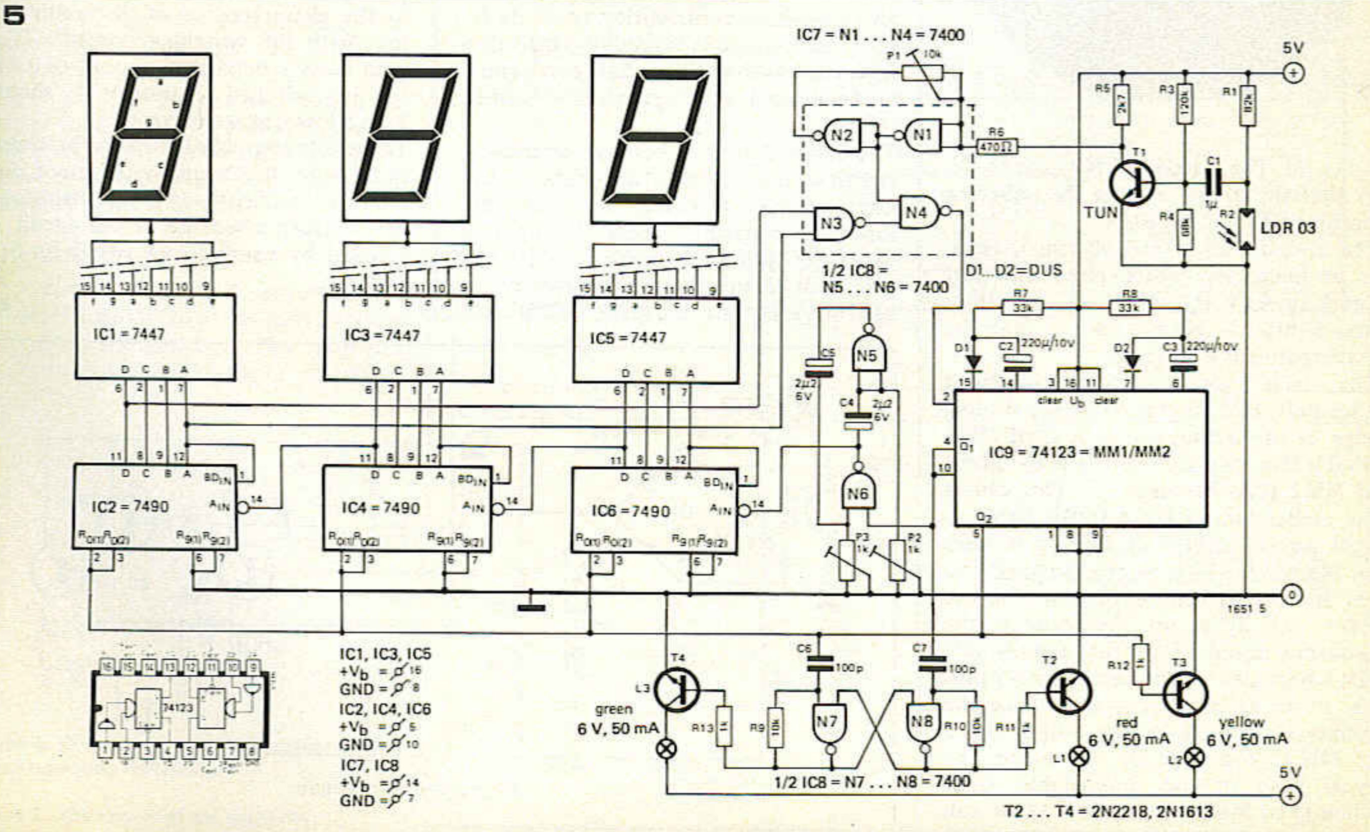
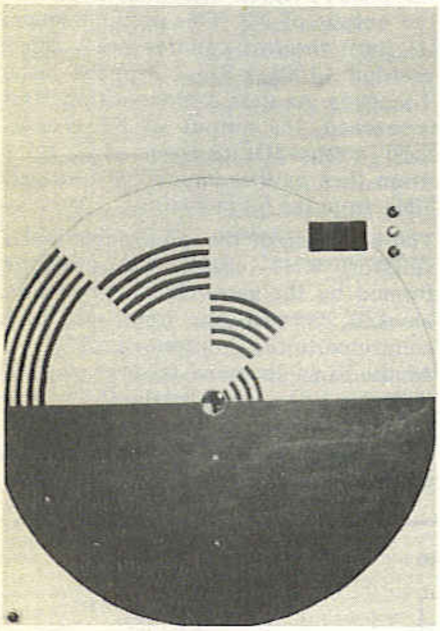




lights up. The output of N7 goes to '0', so that the green lamp in the collector circuit of T4 extinguishes.

The circuit uses a kind of 'traffic light' as an indicator, which gives the start signal (green) and also indicates either that a hit has been made or that the playing time is over (red).

The cycle time of MM1 is about 2 seconds. MM2 is started on the trailing edge of the output signal of $\overline{Q}$ of MM1 (that is after two seconds). The Q-output of MM2 then becomes '1'. This causes the amber lamp of the traffic lights to light up. The set-reset flipflop is reset on the trailing edge of the Q-signal. The red and amber lamp extinguish and the green one lights up. As soon as the $\overline{Q}$-output signal of the first monostable MM1 becomes '1' the oscillator N5 plus N6 starts again. At the same time the counters are reset by the output signal of MM2, and kept at '0' during the cycle time of this monostable. Only when Q of MM2 becomes '0' again, can the counter start counting the pulses of the oscillator. This coincides with the traffic lights changing to green. For 9 seconds it is then permitted to shoot at the target. The cycle described above repeats itself.

The functioning of the traffic light is slightly unconventional. Normally the amber lights gives warning that red is coming up. In this circuit, the amber warns that green is coming up (to indicate that the marksman may 'go' i.e. fire at the target).

Construction

The target is basically a board with a hole in the centre. This hole accommodates a lens with a focal length of about 20 mm. The light sensitive resistor of the hit detector is mounted at the principal focus behind the board. A lens with about the same focal length is mounted in the barrel of the pistol. A diaphragm with a lamp directly behind it is mounted at a distance of about 20 mm from the lens in the pistol barrel. The batteries can be housed in the butt of the pistol, which is a modified toy pistol of an 'automatic' type.

The pistol should be fairly large, so that the components can easily be accommodated inside it (see figure 2). The most realistic results are obtained if the pistol can retain the original cap-firing mechanism to produce a bang when the trigger is pulled.

Conclusion

Besides its original purpose (shooting) this apparatus can also be used for testing reaction speed. The possibility of cheating is then, however present because of the amber warning light and the fixed time cycle.

N. Beun

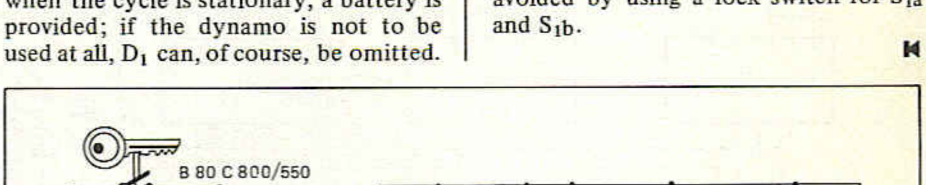
bicycle trafficator

The author does not pretend to present a revolutionary design, but only wishes to give a positive contribution to safety on the road, because in his opinion direction indication is something that leaves much to be desired with cyclists and moped riders.

The design described here is a trafficator circuit which consists of an astable multivibrator and a switching darlington. Since the trafficator must also operate when the cycle is stationary, a battery is provided; if the dynamo is not to be used at all, D_1 can, of course, be omitted.

The flashing frequency is 64 'flashes' per minute and is reasonably constant owing to the characteristics of the multivibrator. With the switching transistor (T_4) used here, a maximum current of 0.4 A can be switched. Transistor T_3 should have a low leakage current.

The whole assembly (including batteries) should be shock and rattle-proof and mounted resiliently in a watertight cabinet. Unauthorised use of the circuit is avoided by using a lock switch for S_{1a} and S_{1b}.



La1, La2 = max. 0.4 A/6.3V

W. Kümmel

30 mhz amplifier

The input threshold voltage of TTL IC's lies between 1.8 and 3 volts. It is often necessary to drive TTL circuits from R.F. equipment with lower output voltages. This simple transistor amplifier can be used to amplify the output of the local oscillator of a receiver or other relatively low-level signals to a level suitable for driving frequency counters and other equipment.

Amplification of signals at frequencies up to 30 MHz without distortion and with a level frequency response requires fairly complex circuitry and may need expensive measuring equipment to set up. For driving digital equipment, however, distortion is less important, and in fact the amplifier described here clips the signal to provide a square wave output. The circuit will operate from a standard TTL (5 V) supply.

Transistors used

Experiments with various R.F. transistors proved unsuccessful due to the tendency of the circuit to 'take-off' into oscillation at umpteen megahertz, or not to work at all with the required supply voltage. Quite by chance a BC109C was soldered into the circuit, which at once performed perfectly. Further experiments showed that a large proportion of BC109C's performed quite happily to above 30 MHz. Tests were carried out on 200 samples of BC107B, BC109C and unmarked 'TUN's', and the results are shown in figure 1. The BC109C gave the best results, with 50% of the specimens tested being usable up to 30 MHz, and 10% still usable at 80 MHz.

The Circuit

The circuit of figure 2 is extremely simple. D1 and D2 limit the input voltage to protect the transistor. The transistor operates as a common-emitter amplifier. The output is fed to a pulse shaper consisting of 2 NAND Schmitt triggers (7413). This produces pulses with a rise time of less than 10 nanoseconds which will ensure reliable operation of the TTL circuits which the amplifier drives.

Construction

One or two points are worthy of note when building the circuit:

1. Lead lengths should be kept short in view of the high frequencies involved, and in particular the output should be as close as possible to the input of the first 7413.
2. A transistor should be chosen with a D.C. current gain of greater than 200 as these are more likely to have a good high-frequency performance.
3. R2 provides D.C. biassing and feedback and should be selected to give a collector voltage of about 1.25 V.
4. The supply filter (R4, C2, C3) is definitely necessary to avoid transients on the supply line driving the amplifier.

If all these points are attended to, the amplifier should operate up to at least 30 MHz with an input sensitivity of 100 mV. Measurements on the local oscillators of receivers can be carried out using the amplifier, although a smaller input capacitor may be required to avoid detuning the oscillator. Alternatively, a direct connection may not be necessary if sufficient signal strength is available. In that case a capacitive coupling may be made by winding a short length of insulated wire around the end of a suitable resistor or capacitor in the circuit under test.

Finally, it should be emphasised that this amplifier is not suitable for analogue amplification of signals, for instance, as an aerial preamplifier, since the signal is clipped. ◼

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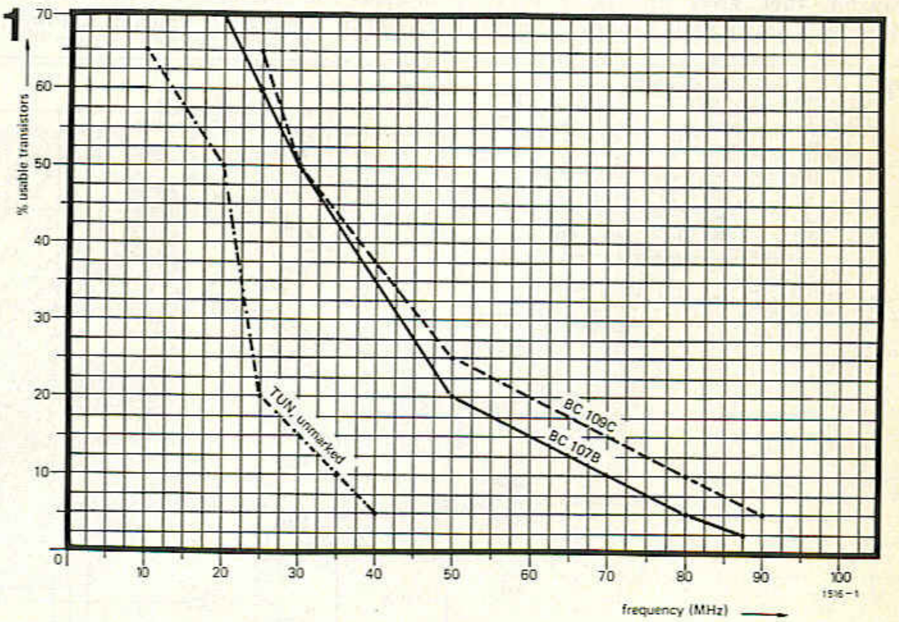

Figure 1. Graph of percentage of usable devices versus operating frequency.

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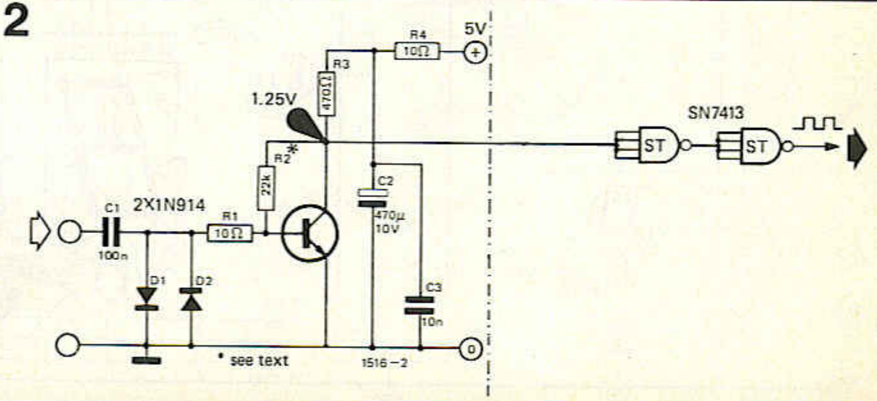

Figure 2. The circuit of the amplifier.

car clock

Although, perhaps, more than enough space has already been devoted to electronic clocks in Elektor, here is a design which is worthy of mention. The Eurosil E1109 IC offers the possibility of a single-chip digital clock operating directly from a crystal reference without any additional divider IC's (unlike the MOSCLOCK 5314). Using this IC a compact clock can be constructed which is eminently suitable as a car clock or portable clock.

The E1109 IC

This COSMOS IC contains all the functions necessary for a 12 or 24 hour clock. It incorporates an oscillator circuit requiring only an external 4.194304 MHz crystal and trimmer capacitor for operation. The display outputs are multiplexed, and common cathode LED displays can be driven via single transistor buffer stages. A 1 second output is available to drive a flashing LED, and an output is also available that gives one pulse every 24 hours. Control inputs are provided in the form of reset (to 0.00), stop, slow and fast forward cycle, for setting the correct time. The circuit will operate on supplies up to +15 volts.

The complete circuit

The circuit of the complete clock is given in figure 1. Although the IC has good noise immunity a supply stabilization circuit is included that incorporates interference suppression, for use in cars. The stabilizer is a simple zener reference driving an emitter follower, T13. However, due to the high current gain of the BC517 (typically 30,000) this circuit gives good regulation with few components. A filter consisting of R1, R2 and C1 suppresses pulses from the car ignition system. C1 should be a low-inductance type of capacitor, preferably ceramic. The stabilizer provides a supply to the clock of about 9 or 10 volts.

The clock may also be powered from the mains by a simple power pack consisting of a transformer, bridge rectifier and smoothing capacitor. The trans-

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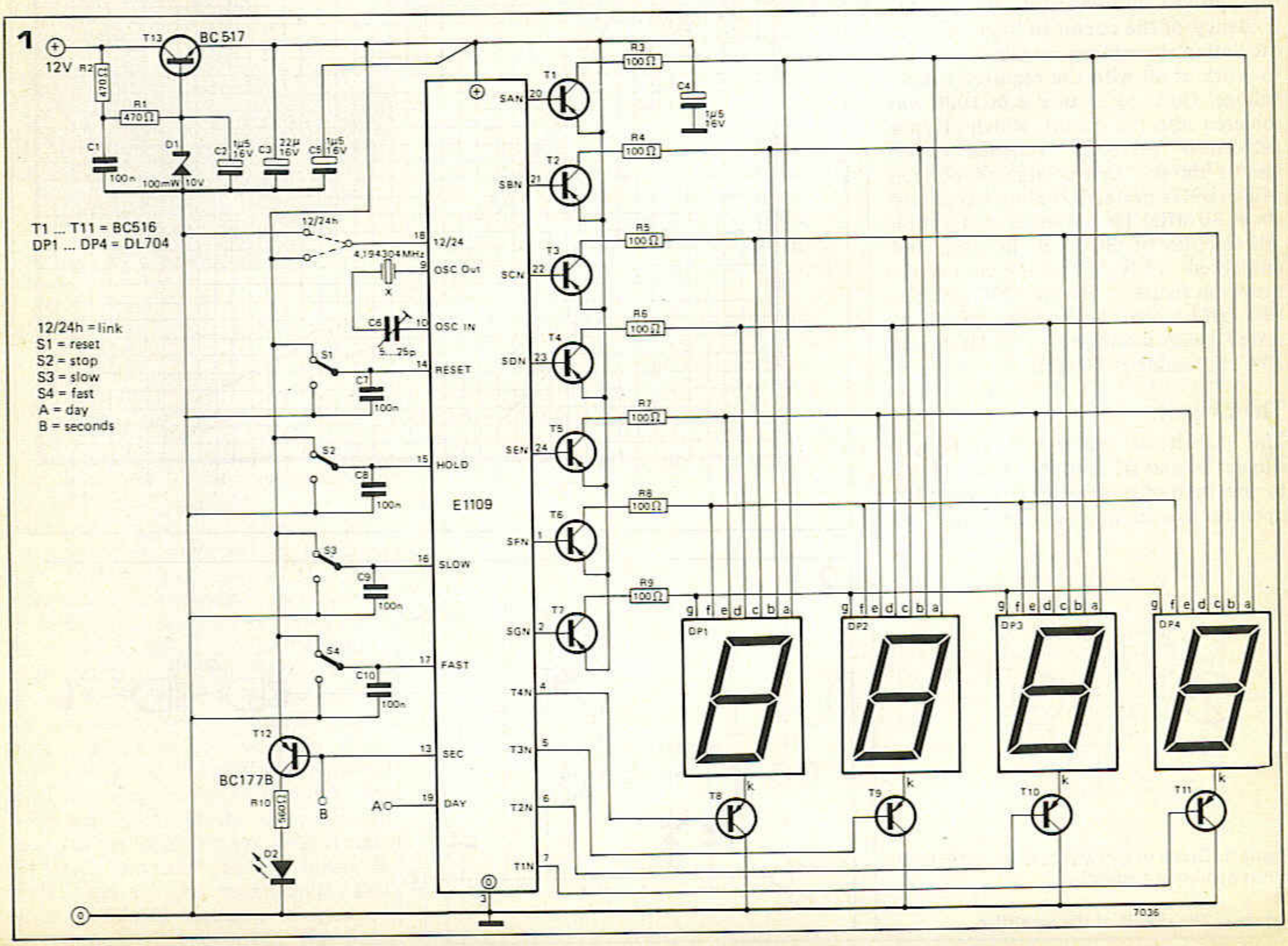

former should have a secondary voltage of about 8 V r.m.s. The output of the power pack can then be connected to the input of the stabilizer on the clock board.

The display outputs of the IC operate on the well-known multiplex system (see 'MOSCLOCK 5314, Elektor Dec. 1974). The multiplex frequency of 1024 Hz is derived, inside the IC, by dividing down the 4.194304 MHz reference frequency. The displays are pulsed sequentially for approximately 61 μs. This means that the segment resistors must be quite low to achieve reasonable brightness.

Since the IC can sink only 0.1 mA at the digit outputs high gain transistors must be used for T8 - T11. For this reason the BC516 was chosen, which has a current gain of typically 30,000. The maximum collector current is also an adequate 400 mA. As the segment drive transistors T1 - T7 carry only one-seventh the current (maximum) of T8 - T11, the BC179C may be a suitable alternative. However, these should be selected for a minimum gain of 400.

The crystal X and C6 are the external oscillator components. The trimmer capacitor is used to adjust the timekeeping of the clock by 'pulling' the oscillator frequency. This may be done by connecting a frequency counter in the period mode to the seconds output pin 13. Direct measurement at the oscillator output should be avoided, as this may load the output and alter the frequency. Alternatively the timekeeping may be adjusted over a longer period using radio or telephone time signals.

The seconds output drives T12 which causes the LED D2 to flash, thus showing that the clock is working. This is, of course, a refinement and may be omitted if the continual blinking of the LED is annoying. The clock may be connected for a 12 or 24-hour cycle by means of pin 18. This is grounded for a

Figure 1. The complete diagram of the car clock, including the stabilized supply. If necessary, the transistors T1. . . T7 can be replaced by types such as the BC 179 C. Each of the latter must then be checked for current amplification factor.

Figure 2. Lay-out and component arrangement of the main p.c.b. The wire bridge serving as the fixed adjustment for 12-hour or 24-hour clock requires extra attention (see text).

Figure 3. The lay-out and component arrangement of the display p.c. board. This board is connected to the main p.c.board by means of the segment resistors (figure 2).

Parts list figure 1

Resistors:
R1,R2 = 470 Ω
R3 . . . R9 = 100 Ω
R10 = 560 Ω

Capacitors:
C1,C7 . . . C10 = 100 n
C2,C4,C5 = 1.5 μ tantalum
C3 = 22 μ, 16 V
C6 = trimmer 5 . . . 25 p

Semiconductors:
IC = E 1109 – Eurosil
T1 . . . T11 = BC 516
T12 = BC 177 B etc.
T13 = BC 517
D1 = zener diode 10 V,100 mW
D2 = LED (TIL209 or similar)

Miscellaneous:
X = 4.194304 MHz-crystal
DP1 . . . DP4 = DL 704 (Litronix) or equivalents
S1 . . . S4 = change-over switches, if required double pole.

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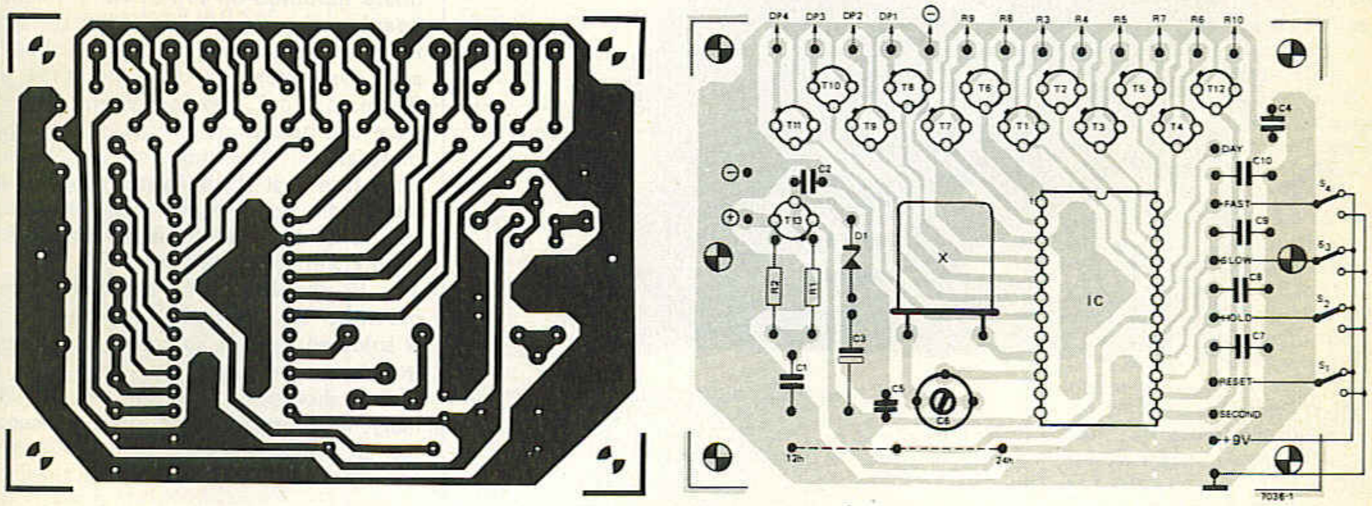

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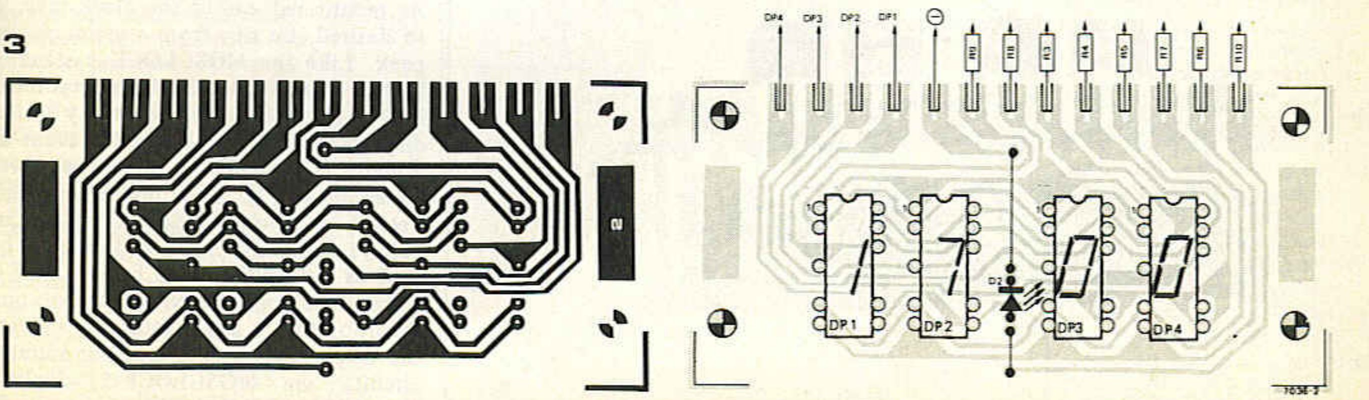

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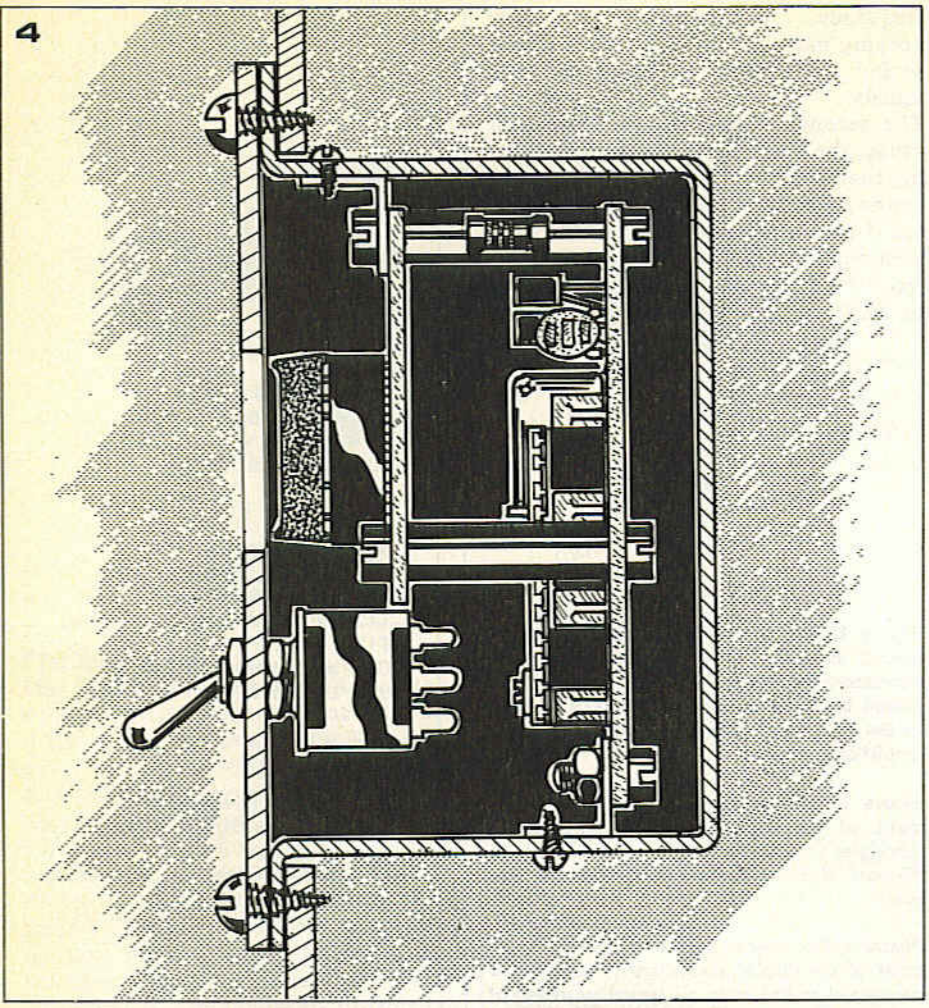
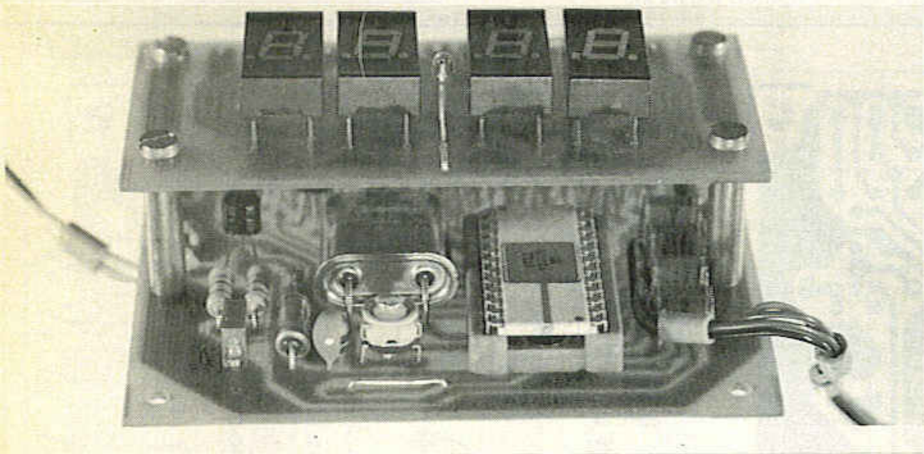
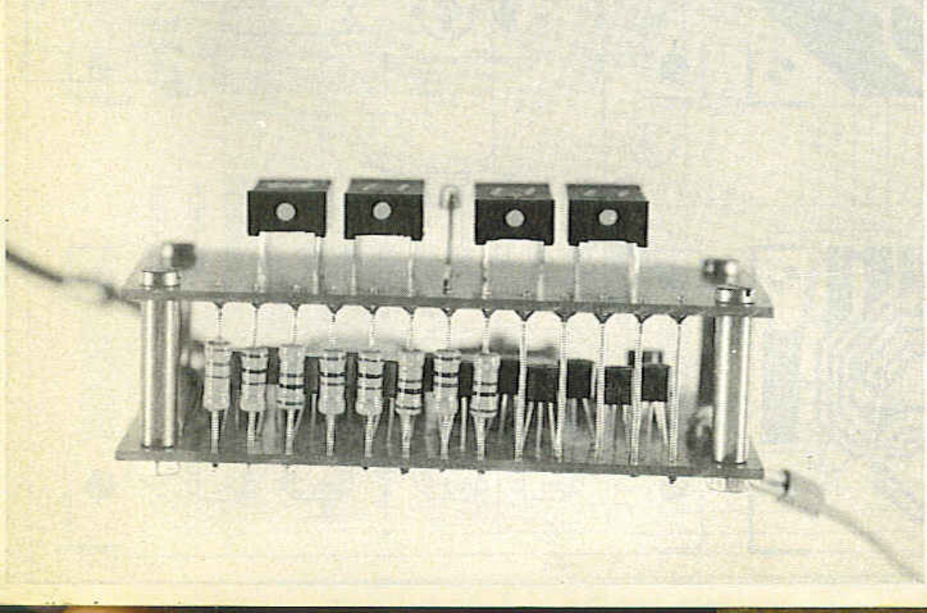


Figure 4. Showing how the main- and display printed circuit boards are interconnected.





12-hour cycle and connected to positive supply for a 24-hour cycle. A link on the board makes this connection to the constructors requirements.

Setting the clock

Grounding the 'reset' input (pin 14) by means of S1 will reset the display to 0.00. Grounding the 'hold' input (pin 15) will stop the clock. S3 causes the minute display to advance by one minute per second, while S3 causes the hours display to advance by one hour per second. C7 - C10 are included to minimise the effects of switch contact bounce. The use of double pole switches with their contacts wired in parallel will also help if needed.

Construction

To keep the finished clock as compact as possible a three-dimensional construction is employed with the display board mounted on top of the main p.c. board, and connected to it by the segment resistors and wire links. The board and component layouts are given in figures 2 and 3, and the general appearance can be seen from figure 4 and the photograph. The link for 12/24-hour operation is at the bottom lefthand corner of the main board. Only one link should be soldered in as otherwise the supply will be shorted out.

The IC should be the last component mounted on the main board and if it is soldered in then an earthed soldering iron must be used. For preference a socket should be used for the IC. Finally, a 500 mA fuse should be connected in series with the positive supply line when the unit is installed in the car.

Variations on the design

As mentioned earlier the clock may, if so desired, be run from a mains power pack. Like the MOSCLOCK a standby battery supply may also be incorporated if it is arranged that the supply to the displays is switched off in the event of a mains failure. (This reduces the power consumption to the few microamps needed to power the COSMOS circuitry). Alternatively, the clock may be used as a travelling clock by powering it from a rechargeable NiCd battery, and incorporating a pushbutton to activate the display when required. For suitable circuits see MOSCLOCK 2, Elektor June 1975.

MARKET

COS/MOS opamp

The CA3130 series of operational amplifiers, which RCA have introduced, offer a combination of the advantages of COS/MOS and bipolar transistors. A very high input impedance is achieved by the use of P-MOS (P-channel MOS) FETs in the input stage, while a large output voltage swing is made possible by the use of a COS/MOS transistor pair for the output amplifier.

The CA3130 is supplied in a TO-5 housing. Type CA3130T has normal leads, while those of type CA3130S are bent into a DIL configuration. Three variants of the electrical specification are available:

CA3130T and CA3130S are the standard versions;

CA3130AT and CA3130AS have improved input specifications;

CA3130BT and CA3130BS are better still.

Figure 1 shows the connections for the T versions. In the S versions, connections 1, 2, 3 and 4 lie along one line while 5, 6, 7 and 8 lie along the other line.

The CA3130 can work off asymmetrical power supplies from +5 to +16 V, or from ±2.5 to ±8 V symmetrical supplies.

Figure 2 shows the block diagram of the CA3130. Input pins 2 and 3 can be driven down to 0.5 V below the negative supply (pin 4). In many applications the output can be swung very nearly positive or negative supply level. For these reasons, the CA3130 is ideal for use with a single supply.

Three class-A amplifier stages (shown as B, C and D in figure 2) provide the overall gain of the CA3130. A bias circuit (A) provides two voltages for the first and the second stage.

Pin 8 can be used for phase compensation, and/or to strobe the output stage into quiescence. When pin 8 is connected to the negative supply (pin 4), the output voltage at pin 6 rises almost to that of the positive supply voltage on pin 7. This condition of essentially zero current drain in the output stage under the strobed 'off' condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g. when the amplifier is used to drive COS/MOS digital circuits).

Input stages

The internal circuitry of the CA3130 is shown in figure 3. The circuit has a differential input stage with P-MOS field-effect transistors (T6 and T7), working into a mirror-pair of bipolar transistors (T9 and T10) which function as load resistors.

The output voltage of T10 is used to drive T11 in the second stage.

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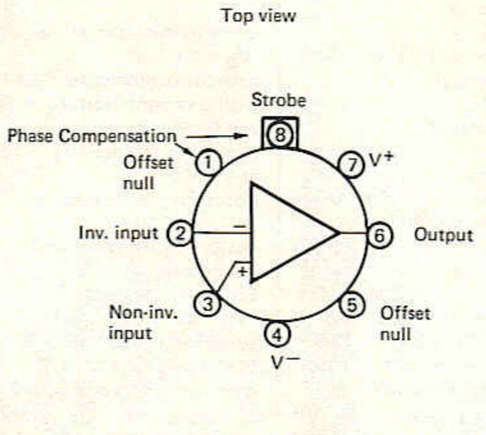

Case connected to pin 4

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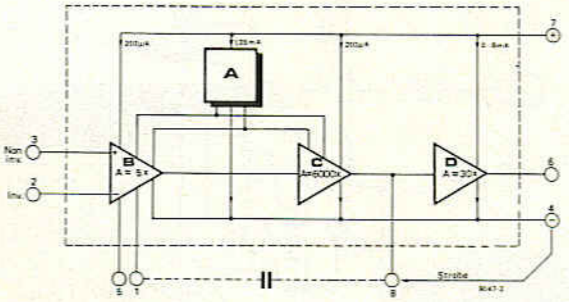

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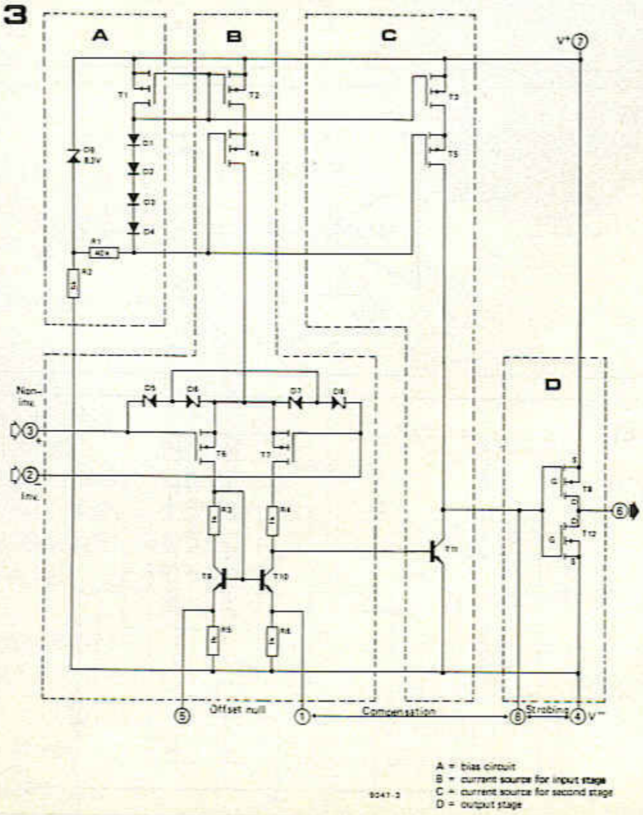

Offset nulling, when desired, can be effected by connecting a 100 kΩ potentiometer across pins 1 and 5, with the slider connected to pin 4.

Cascode-connected P-MOS transistors T2 and T4 are the constant-current source for the input stage. The bias circuit for the current source will be described later.

The diodes D5-D7 provide protection for the gate against high-voltage transients due, for example, to static electricity.

Second stage

Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor T11 and its cascode-connected load resistance provided by P-MOS transistors T3 and T5. The source of bias potentials for these P-MOS transistors will be described later. Miller-effect compensation (roll-off) is accomplished by simply connecting a small capacitor between pins 1 and 8. A 47 pF capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit

At total supply voltages somewhat above 8.3 V, resistor R2 and zener diode D9 serve to establish a constant voltage across the series-connected circuit, consisting of resistor R1, diodes D1 to D4 inclusive, and P-MOS transistor T1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias of about 4.5 V for P-MOS transistors T4 and T5 with respect to pin 7. A potential of about 2.2 V is developed across diode-connected transistor T1 with respect to pin 7 to provide gate bias for transistors T2 and T3. It should be noted that T1 is 'mirror-connected' to both T2 and T3. Since transistors T1, T2 and T3 are designed to be identical, the approximately 200 µA in T1 establishes a similar current in T2 and T3 as constant-current sources for both the first and second amplifier stages, respectively. At supply voltages somewhat less than 8.3 V, the zener diode becomes non-conductive and the potential, developed across series-connected R1, D1 ... D4, and T1, varies directly with variations in supply voltage. Consequently, the gate bias for T4, T5 and T2, T3 varies in accordance with supply voltage variations. This variation results in deterioration of the power supply rejection ratio (PSRR) at total supply voltages below 8.3 V. Operation at total supply voltages below about 4.5 V results in seriously degraded performance.

market

Output Stage

The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors T8 and T12 operating in the class-A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

Applications

In figure 4 the CA3130 is used as a voltage follower. The bandwidth is 4 MHz and the slew rate is 10 V/µs.

Figure 5 gives the circuit of a CA3130 as a peak detector for positive voltages. It should be noted that, because of internal capacitances, the bandwidth for small signals is less than for large signals. For a 6 V peak-to-peak signal, the 3 dB bandwidth is 1.3 MHz, while for a 0.3 V peak-to-peak signal the 3 dB bandwidth is 240 kHz.

In conclusion, figure 6 shows a circuit in which a CA3600E is used to boost the output power of the CA3130. The current consumption of a CA3600E as a class-A amplifier is 20 mA with a supply potential of 15 V. This arrangement increases the current-handling capacity of the CA3130 output stage by about x 2.5. With feedback, the closed-loop gain of the circuit is 48 dB. The 3 dB bandwidth is about 50 kHz. Output power is 150 mW with a total harmonic distortion of 10%.

Figure 1. Connection diagram for the CA3130T.

Figure 2. Block diagram of the CA3130 series of opamps.

Figure 3. Basic circuit of the CA3130 series of opamps.

Figure 4. Voltage-follower circuit for a CA3130.

Figure 5. Peak positive detector circuit for the CA3130.

Figure 6. Increasing the output power of a CA3130 by connecting a CA3600E.

Table

Typical values for the CA3130 COS/MOS opamp.

Supply voltage	+5 V ... +16 V or ±2.5 V ... ±8 V
Input offset voltage (V_b = ±7.5 V)	8 mV
Input offset current (V_b = ±7.5 V)	0.5 pA
Input resistance (V_b = ±7.5 V)	$1.5 \times 10^{12}\Omega$
Input quiescent current (V_b = ±7.5 V)	5 pA
Input-voltage range (V_b = +15 V)	−0.5 V ... 12 V
Maximum output voltage (V_b = +15 V: R_L = 2 k)	13.3 V
(V_b = +15 V: R_L = ∞)	15 V
Maximum output current (V_b = +15 V) I_{source}	22 mA
I_{sink}	20 mA
Open-loop gain (V_b = +15 V) when V_{out} = 10 V_{pp} and R_L = 2 k	110 dB
Unity-gain crossover frequency (V_b = ±7.5 V) without compensation	15 MHz
with compensation (C_c = 47 p) and 0 dB gain	4 MHz
Input capacitance (V_b = ±7.5 V) at 1 MHz	4.3 pF
Common mode rejection (V_b = +15 V)	90 dB
Power supply rejection (V_b = ±7.5 V)	32 µV/V
Equivalent input noise (V_b = ±7.5 V) when R_s = 1 M; bandwidth = 200 kHz	23 µV
Slew rate (V_b = ±7.5 V) with open loop and C_c = 0	30 V/µs
with closed loop and C_c = 56 p	10 V/µs

These values are valid for an ambient temperature of 25°C.

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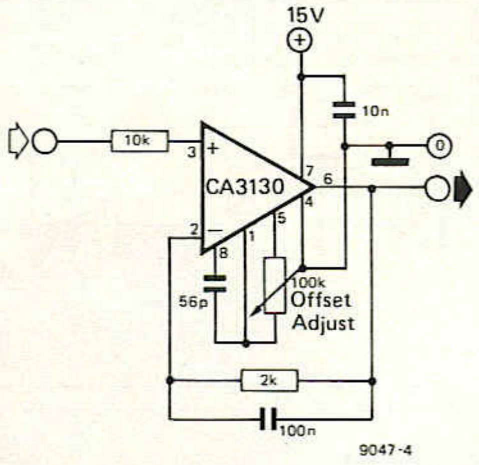

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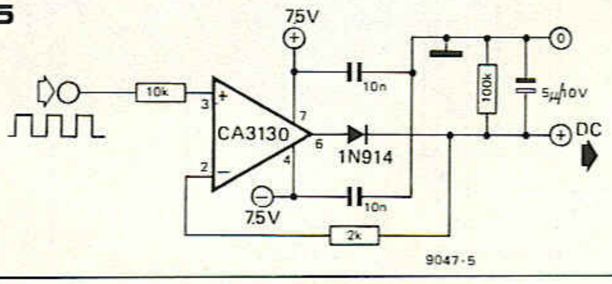

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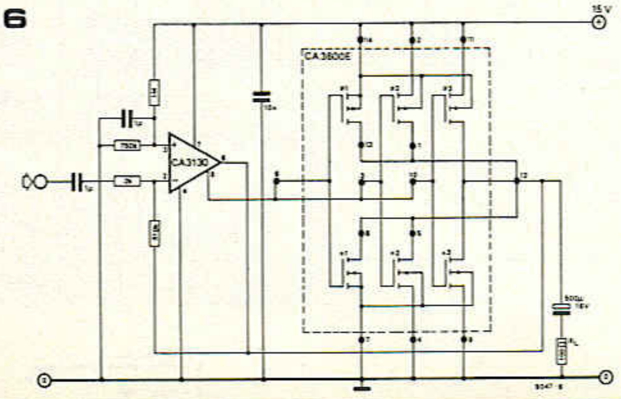

5½ digit panel meter

Digilin, Inc., of Burbank, California, announce the introduction of a 5½-digit panel meter, Model 2552, offering .01% accuracy, four counting modes and 100% overranging. Direct readout in measurement units, e.g., lbs, CFM, PSI, makes the new instrument suitable for monitoring of weight, pressure, flow or other industrial processes.

Model 2552 permits count by 10's, 5's, 2's and 1's. Maximum readout in the 'count by 10's mode', including overrange, is 199,990, with the least significant digit a 'dummy' zero. Full scale readout for count by 5's, 2's and 1's is 50,000, 20,000 or 10,000 respectively, plus 100% overrange. A Beckman (Sperry-type) display is utilized.

Counting modes and decimal point location are selected by changing jumper wires on the rear connector. A hold function is also available at the connector. Automatic polarity, TTL compatible BCD outputs, display storage and a sealed case are other features. Maximum resolution is 100 µV per count (1 µV resolution is available as an option.)

Other major specifications: temperature stability (0 to +50°C) is better than ±.005% full scale per °C. NMNR is 30 dB at 60 Hz. CMNR is 100 dB at DC, 80 dB at 60 Hz. Input impedance is greater than 100 megohms and bias current is typically 20 nA (50 nA maximum). The panel opening required is a compact 3.74"W x 2.05"H.

F-Dyne electronics establishes international division

F-Dyne Electronics Company of Bridgeport, Connecticut has established an International Division to sell their precision capacitors to the overseas market. The new international division will be located at 2200 Shames Drive, Westbury, L.I., New York 11590. Telex 961474.

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PUBLISHER'S ANNOUNCEMENT

Because of the very strong demand for Elektor to be made available through bookstalls and newsstands, arrangements have been made for Elektor 7 to be on sale throughout the UK on 17 October.

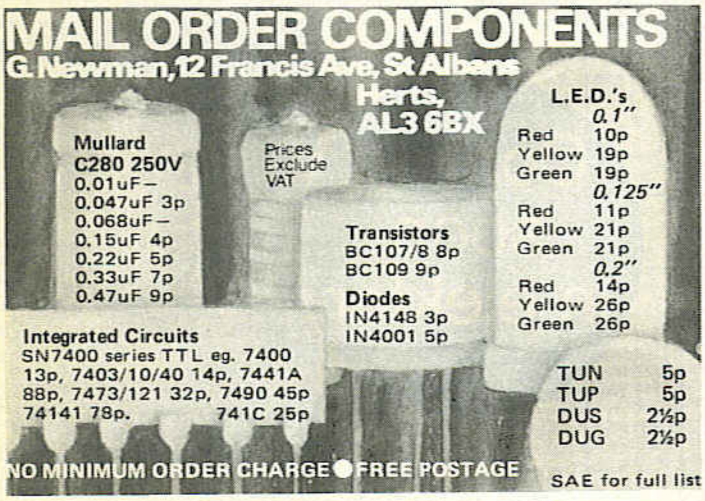
To comply with the timing arrangements necessary for this, we will have to re-date our magazines from October on. This issue is dated 'September', as planned, but Elektor 7 will be dated 'November'. In effect, there will be no issue dated 'October', although Elektor will be published on a monthly schedule from now on.

For our subscribers, the effects will be:

- the publishing dates will not be affected; the next issue (dated 'November') will be sent to subscribers during the first few days of October.
- subscribers will, of course, still receive magazines up to and including Elektor 9 this year, even though Elektor 9 will be dated 'January 1976'.
- when subscriptions are renewed for 1976, the invoices will be based on the subscription rate for February up to and including December 1976.

For non-subscribers, the effect will be that Elektor 7 will be on sale at newsagents and stationers throughout the UK on 17 October, and future issues will be available at the same place on the third Friday of every month. Place your order with your newsagent now to avoid disappointment. Of course, Elektor will continue to be available from leading electronic component suppliers throughout the UK and also directly from the publishers.

We apologise for any inconvenience that may be caused by the re-dating, but we feel that the advantages more than compensate for any disadvantages.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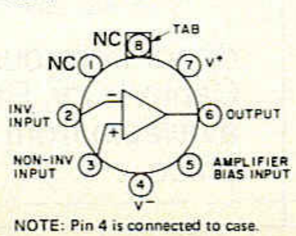
THE MISSING LINK

Modifications to
Additions to
Improvements on
Corrections in
Circuits published in Elektor

In the pinning list for linear ICs (Elektor 'Summer circuits', p. 775), pins 1 and 8 of the CA3080 are shown as 'phase compensation'. This is in accordance with the 1975 edition of the RCA databook, but it is not correct ... These pins are not connected, and should be labeled 'NC'.



NOTE: Pin 4 is connected to case.

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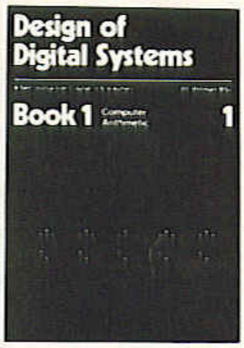

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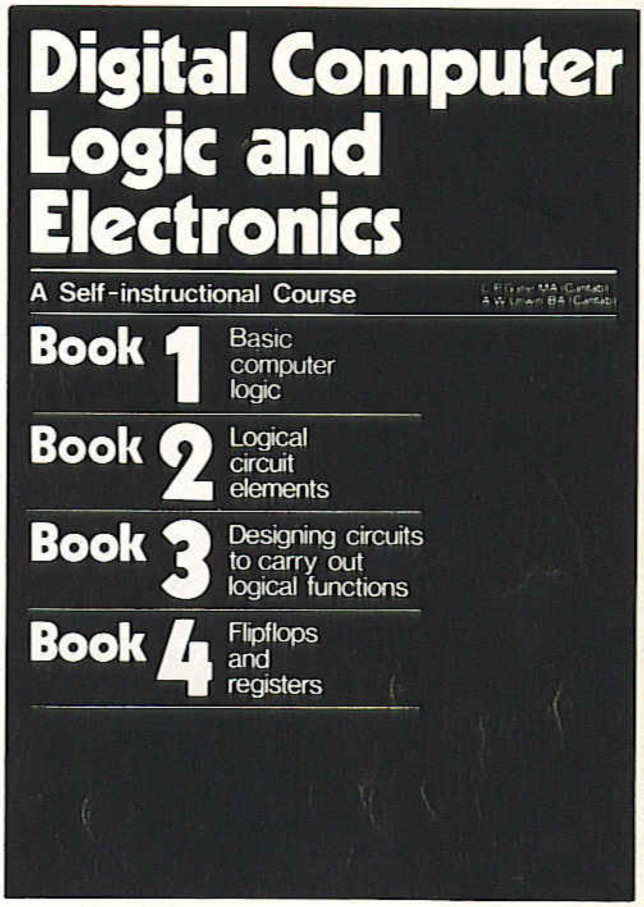
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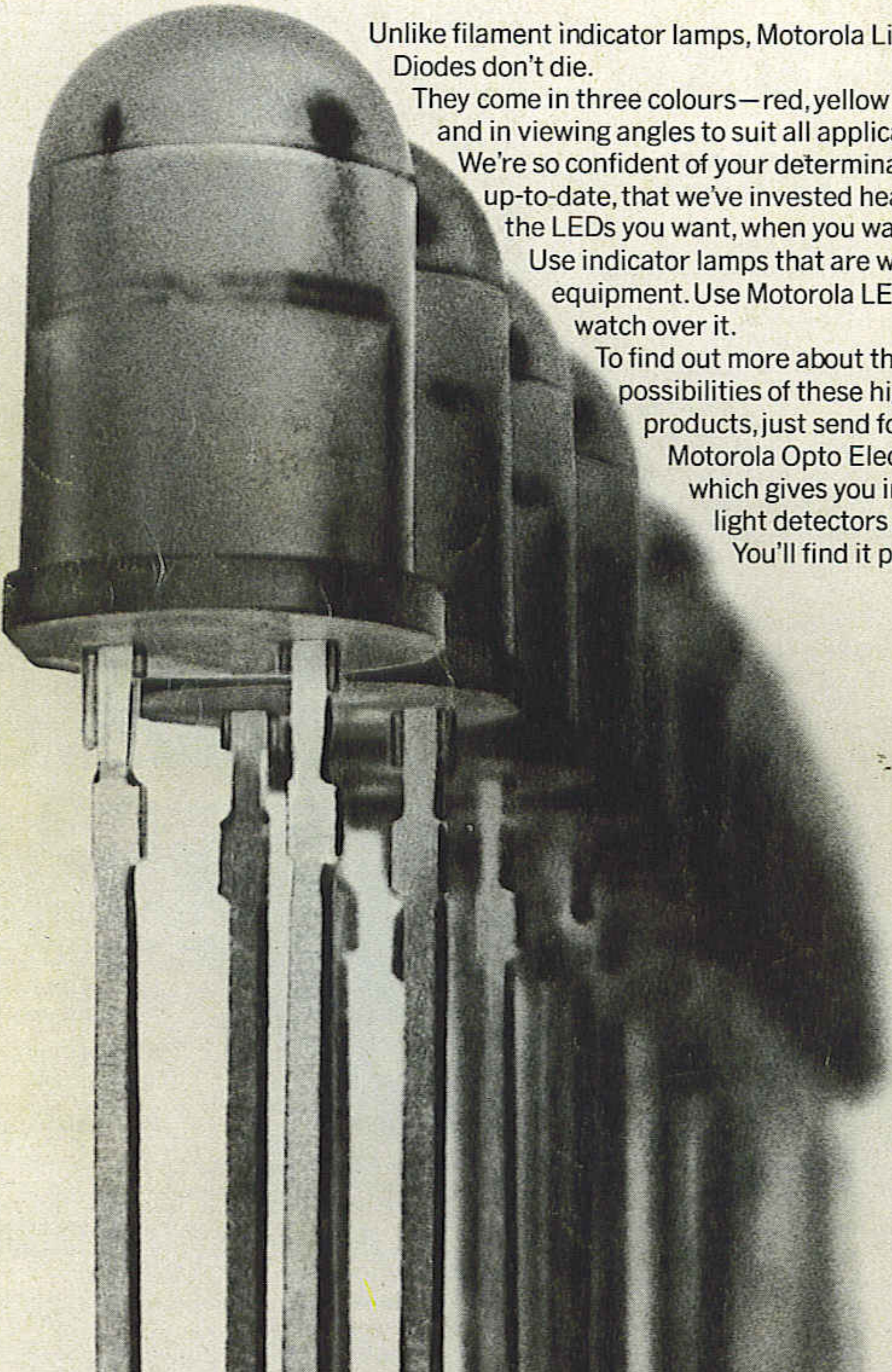

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